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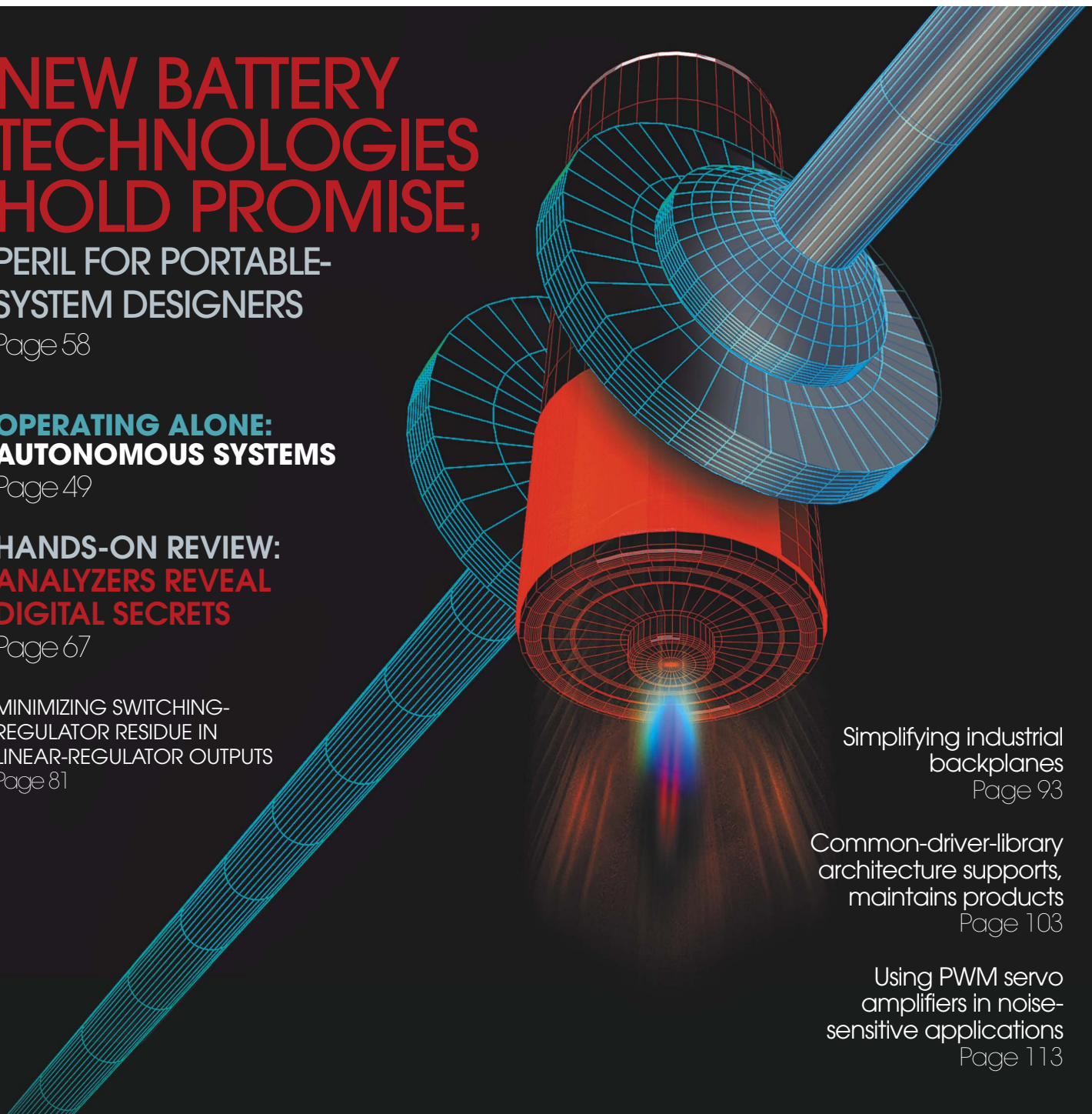

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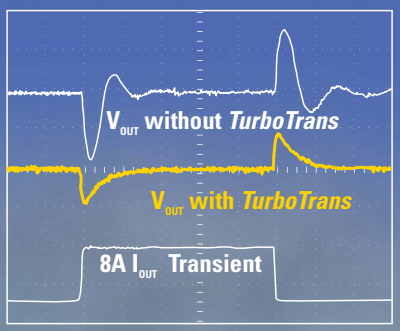

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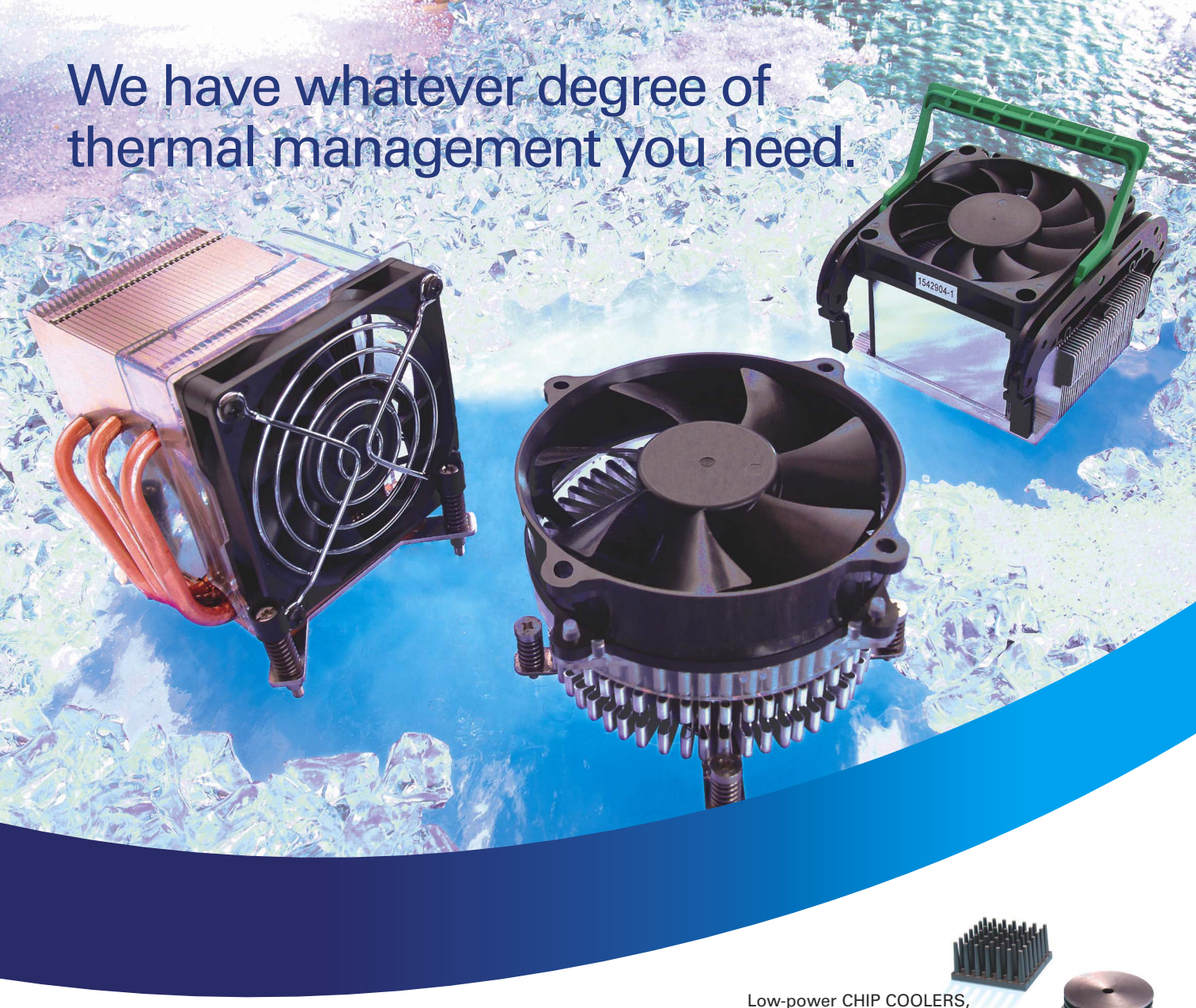

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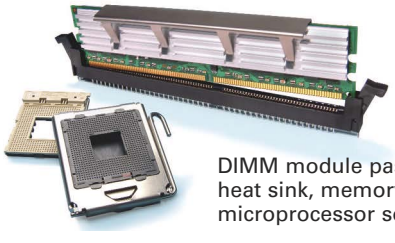

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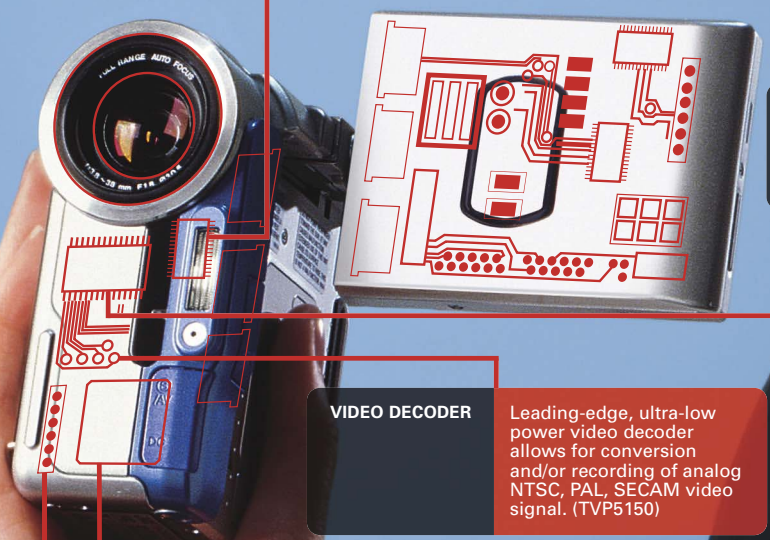

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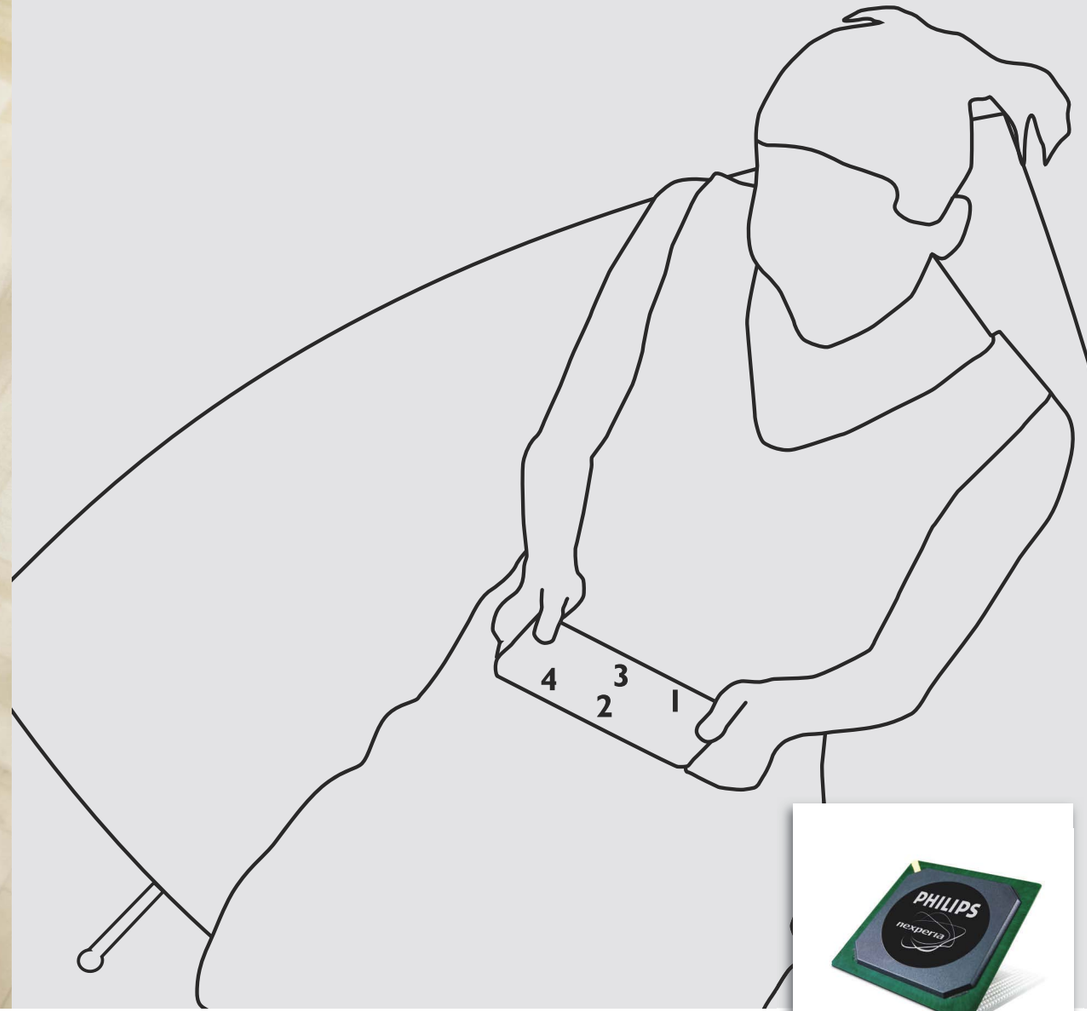

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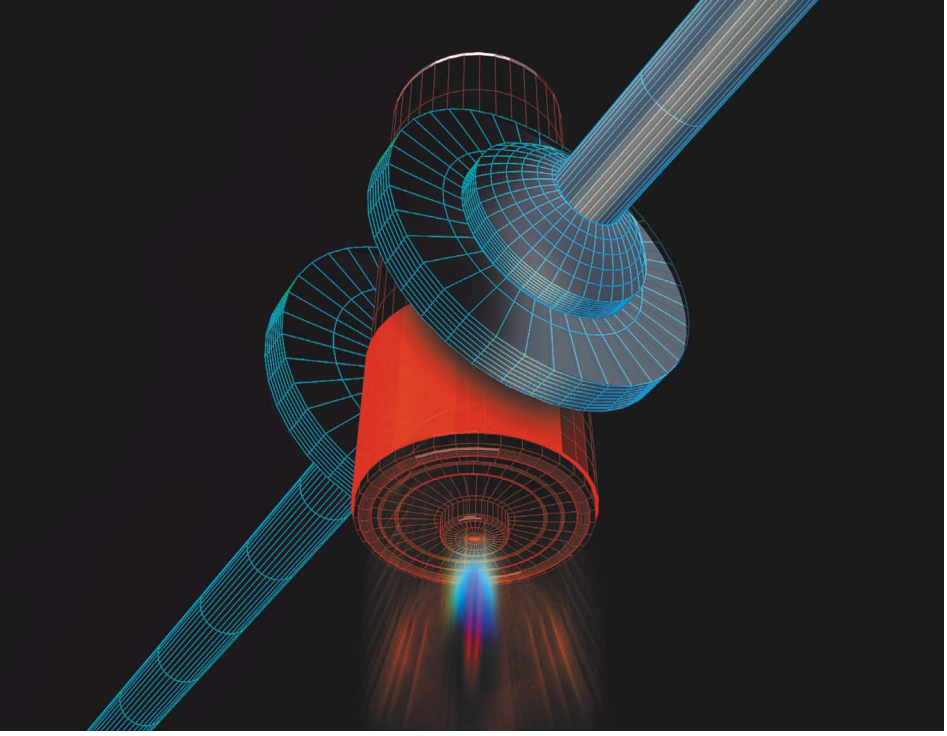

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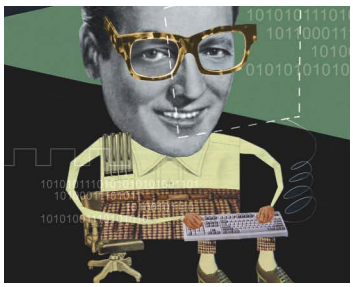

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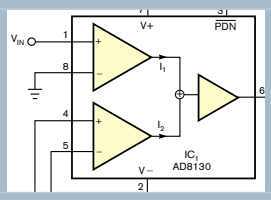

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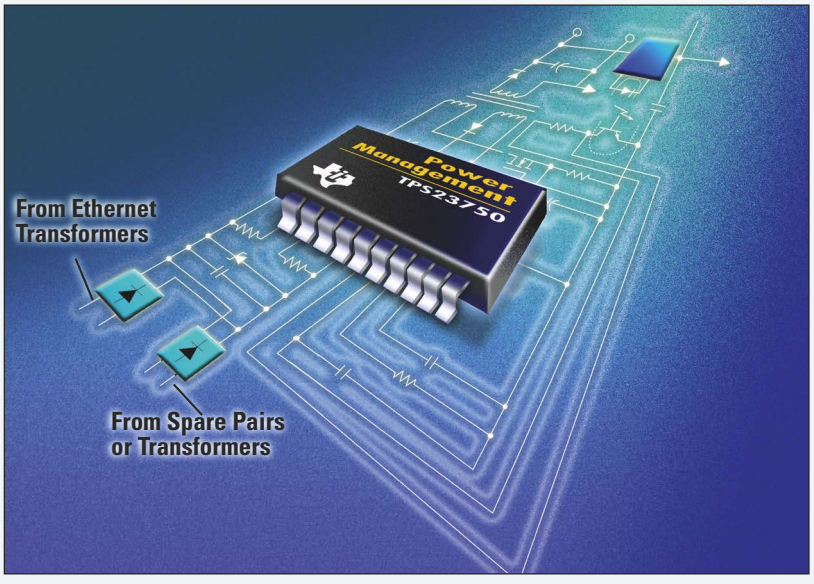

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TPS2377	100V	Legacy	0.6	PG Pin	8-Pin SOIC, TSSOP
TPS23750	100V	IEEE 802.3	0.7	Integrated Controller	20-Pin HTSSOP
TPS23770	100V	Legacy	0.7	Integrated Controller	20-Pin HTSSOP

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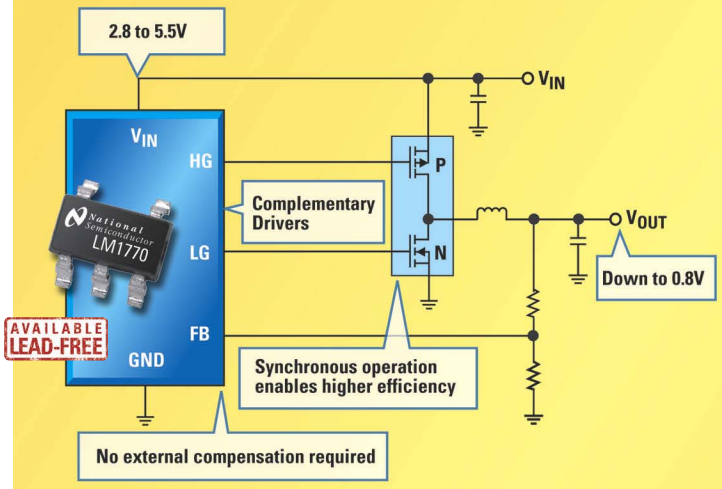
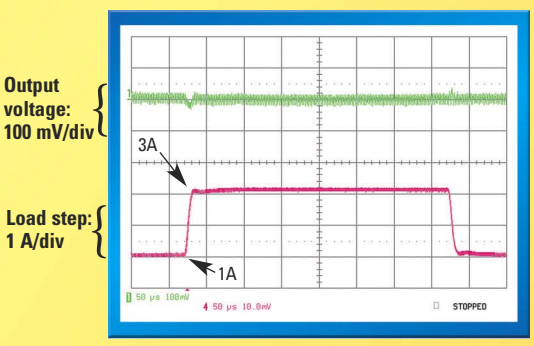


Transient Response



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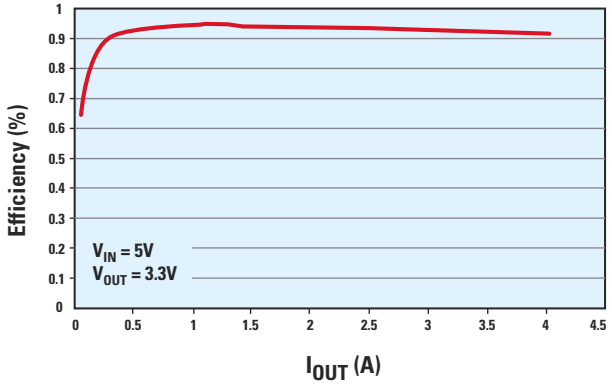

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A new EDA startup, Pyxis Technology Inc, is coming out of stealth mode and says it will release mid next year a design-for-manufacturing-savvy digital-IC router that will lead the next retooling in the implementation segment of EDA.
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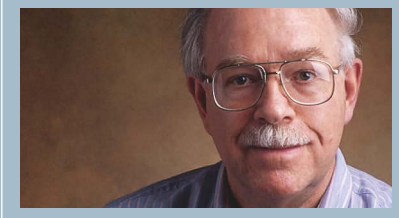

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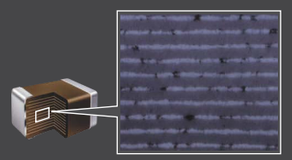

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BY MAURY WRIGHT, EDITOR IN CHIEF

Are cell-based ASICs going away?

I can't count the number of conference sessions I've attended at which a speaker shows a market graph of ASIC-design starts. This chart, which is seemingly in every PowerPoint deck, shows a peak in these starts over the past few years with a dramatic drop in starts taking place in the next few years. I don't buy these projections.

Cost drives the pessimistic projection of ASICs in the future. A few years ago, everyone started talking about the cost of mask sets, and they are expensive. More recently, it's been the cost and time associated with verification that people often cite as the dominant cost component. In any event, the costs associated with 90-nm and finer geometry ASICs mean that only high-volume products justify the investment.

But what is high volume—especially in the age of 90-nm chips and 300-mm wafers? Smaller dice and larger wafers change the definition. All of a sudden, the demand for a product such as a communication chip for a router or switch, which many consider a high-volume product, can't fill a single tub of wafers per year. Outside PC processors, graphics processors, cell-phone basebands, and memory, not many ICs qualify as high volume on state-of-the-art process lines.

I recently attended the SOC (system-on-chip) conference presented by Savant. The "death-of-the-ASIC" chart appeared in several presentations, and the projected ASIC replacement was generally the structured or the platform ASIC. Such products combine preverified layers of a chip design with a minimal amount of mask processing for customization. Presumably, the result is something almost as dense as a cell-based ASIC with much lower NRE (nonrecurring-engineering) cost.

At the conference, Fujitsu, LSI Logic, Altera, eASIC, and others each spun its ASIC-replacement story. Most, however, failed to address the problem of volume production on state-of-the art lines. Only eASIC has an answer for the volume issue. CEO Ronnie Vasishta points out that, because the eASIC FlexASIC products require only the top via layer be customized, the company can manufacture multiple designs on one wafer. Vasishta claims that the company's Direct-Write eBeam technology, which handles the top layer, is cost-effective even for mid-volume chips and that, as volumes grow, a design can move to a mask layer to handle the interconnect.

Cost drives the pessimistic projection of ASICs in the future.

Although eASIC has an interesting technology, I'm still not sure that I see it as an ASIC replacement. My guess is that it's less silicon-efficient than other structured-ASIC choices. In fact, eASIC may win more business as an IP (intellectual-property) provider of configurable-logic blocks to other IC vendors than as a fabless semiconductor company. The company's greatest success story to date came through a customizable IP block that it sold to STMicroelectronics, which used the eASIC IP to make a cell-based SOC design customizable.

At the end of the day, all of the analyst projections for declining ASIC starts and all of the structured-ASIC players rely on a common theory. Presumably, the move toward SOCs—more specifically, more functions integrated on a single die—requires that mainstream ASIC designs—or structured-ASIC designs replacing cell-based ASICs—must move down the Moore's Law curve to 90-nm and finer geometries. But do they? Clearly, examples exist of SOCs at the 180-nm node. I recently visited with Fujitsu, and the company's most recent high-profile product launch is an SOC for WiMax applications. Fujitsu produces that chip in a 180-nm process, although the company is eyeing 90 nm for the next-generation chip.

In the past, almost all chip designs moved through process reductions to lower cost through smaller dice while realizing performance gains and reductions in power. Today, only truly high-volume ICs, extremely large dice, or both realize a cost benefit from a 90-nm process and 300-nm wafers. Most ASIC designs today are at 180-nm and less dense geometries. These less dense ASICs have driven the recent peak in ASIC design starts. I believe that most ASIC designs will stay at these relatively low-cost geometries unless performance mandates a different choice. The payoff is in both affordability of the design upfront and fewer problems with static power consumption due to current leakage. That potential payoff may yet make those ASIC-design-start graphs look vastly different. EDN

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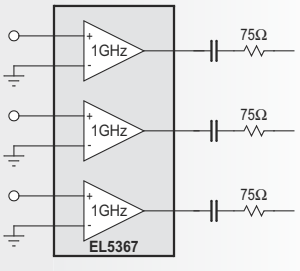

Part No.	BW (MHz)	SR (V/µs)	I_S (mA)	A_V (min) (V)	I_{OUT} (mA)	V_{OUT} (V)
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EL5362	500	2500	1.5	1	100	±3.6
EL5364	600	4200	3.5	1	140	±3.8
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EL5160/1	1	200	1700	0.75	1	70	±3.4	5
EL5162/3	1	500	4000	1.5	1	100	±3.6	5
EL5164/5	1	600	4700	3.5	1	140	±3.8	3.5
EL5166/7	1	1400	6000	8.5	1	160	±3.8	5
EL5260/1	2	200	2000	0.75	1	70	±3.4	5
EL5262/3	2	500	2500	1.5	1	100	±3.6	5
EL5462	4	500	2500	1.5	1	100	±3.6	5

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- Almost zero overshoot
- Low power consumption

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EL5100/1	1	300	2200	10	2.6	100	±3.4	5
EL5102/3	1	400	2200	6	5.2	150	±3.7	5
EL5104/5	1	700	4500	14	9.5	160	±3.8	5
EL5202/3	2	400	2200	6	5.2	150	±3.9	5
EL5204/5	2	700	3000	10	9.5	160	±3.8	10
EL5300	3	200	2200	10	2.5	100	±3.4	4
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EL5304	3	700	3000	10	9.5	160	±3.8	10

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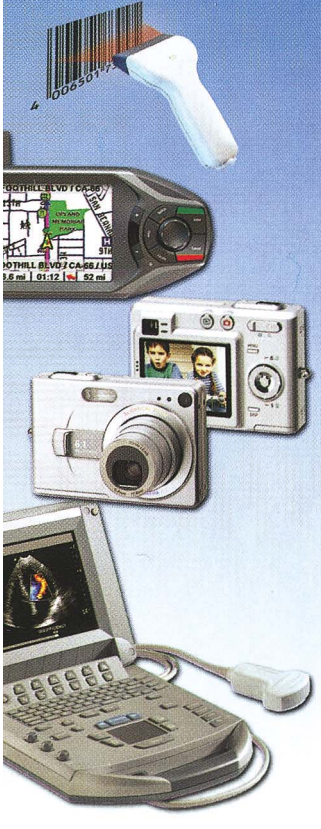


Advanced Topics in Powering FPGAs

— By Tushar Dhayagude, Marketing Manager, Power Management Products

Application	Input Voltage/ Source	Space Constraint	Operational and Light Load Efficiency
Battery Operated/ Portable	1.8V to 5.5V AA batteries, Lithium Ion cells	Severe	High efficiency, low quiescent current
Consumer (DVD, Set-top Boxes, DVR)	4.5V to 36V Wall-plug	Moderate	Low operating efficiency acceptable
Automotive	7V to 45V Battery	Minimal	Low quiescent current
Networking (Routers, Switchers)	3.3V to 12V Brick output	Moderate	Moderately high efficiency
Industrial (Automation, Process Control)	12V to 36V	Minimal	Low

Table 1. Power Requirements for Popular FPGA Applications

FPGAs have established themselves as the most flexible and reconfigurable intelligence in applications from networking and telecommunications equipment to industrial and automotive segments. More recently FPGAs have proliferated into consumer devices such as set-top boxes, DVD recorders, and video games. But future growth in FPGA usage will come from their adoption into portable devices such as GPS, medical, instrumentation, and consumer devices.

Why are the designers of portable and handheld devices turning to FPGAs now? It is because, as process technology has improved, manufacturers have made huge strides in reducing the power consumption, cost, and footprint of FPGAs. But as FPGAs proliferate into portable devices, power management becomes an increasingly challenging issue from a system perspective.

Power supply requirements are important because issues such as input voltage source, complex start-up conditions, transient response, sequencing, have to be addressed. Multiple voltages are required to power an FPGA: "Core" voltage (0.9V to 2.5V), I/O voltage (2.5V to 3.3V) and another low-noise, low-ripple voltage for auxiliary circuits (2.5V or 3.3V typ.). Furthermore, when FPGAs operate from batteries, system efficiency and battery life become crucial.

NEXT ISSUE:

RF Power Efficiency Optimization

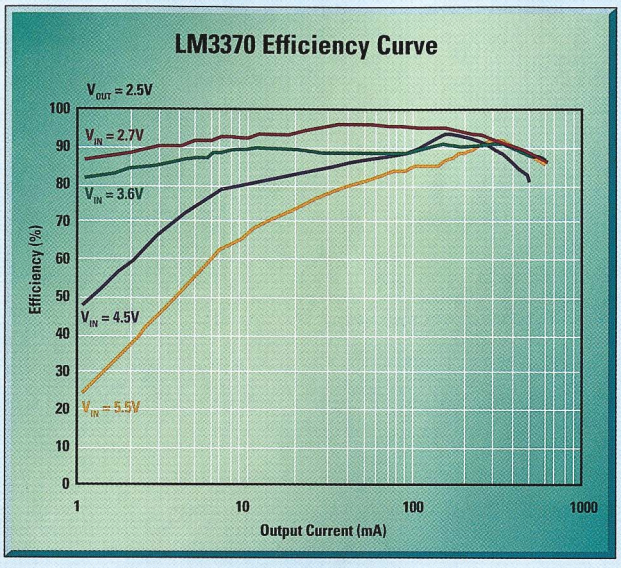
National Semiconductor

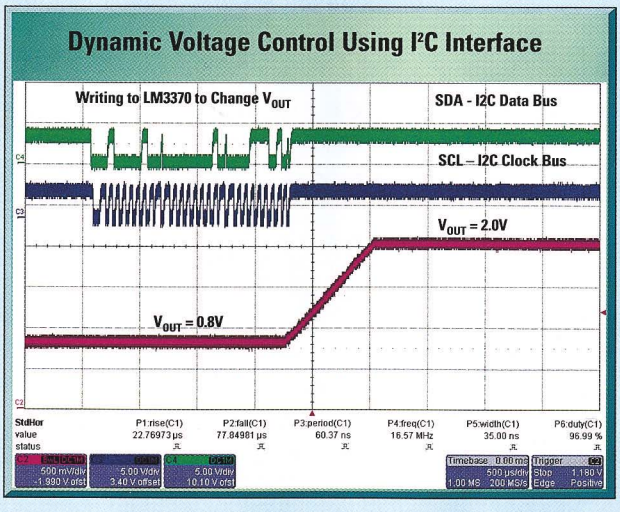
Dual 600 mA Step-Down DC-DC Converter with I²C Interface

Highest Efficiency LM3370 Maximizes Processor Performance through Dynamic Voltage Scaling

Features

- Highest efficiency: PFM-PWM mode control, 85% at 500 µA, >90% at 200 mA
- I²C interface for dynamic voltage scaling, mode control, on/off functions
- Lowest Iq in the industry (<20 µA) enables longer standby times
- Independent mode switching between auto and forced PWM mode
- Two enable pins for power sequencing
- Spread spectrum function to reduce switcher noise — ideal for RF systems
- Power-on-reset to protect the end application from sudden power losses
- V_{IN}: 2.7V to 5.5V, V_{OUT}: I²C programmable
- Integrated solution for optimal solution size





Applications

Ideal for low-power FPGAs, CPLDs, and applications processors

Product Highlight:

Highest efficiency maximizes battery life and I²C voltage control enhances processor performance

Advanced Topics in Powering FPGAs

We discussed some of the basics of powering FPGAs in Power Designer #102[1]. Now we will examine some advanced topics in FPGA power management with a special focus on portable systems, including:

- System-level challenges in powering FPGAs in portable devices
- Monotonic rise of core voltage
- Voltage scaling and back body biasing of FPGAs to improve efficiency

System-Level Challenges

Irrespective of the FPGA being used, the end system dictates the power supply challenges. For example, in a DVD recorder with satellite broadcast, dozens of power rails may be required in addition to powering the FPGA. In such a system, power supply size and efficiency may not be a premium, but very low cost is. Conversely, in battery-operated systems, efficiency overrides all other requirements. ***Table 1*** shows some popular end applications for FPGAs and their power challenges.

In portable devices, efficiency during both active and stand-by modes of operation is of paramount importance. Efficiency directly affects battery life and the duration of usable operation. The input voltages for battery-powered systems range anywhere from 1.8V to 5.5V. The most common sources of power are either 2 AA or single Li-Ion cell batteries whose voltage ranges from 3V to 4.2V. Operating currents are typically less than 1.5A, with most applications requiring less than 600 mA. Although there are general guidelines for using the right step-down solution for powering FPGAs (See Power Designer #102[1]), portable devices mandate that high efficiency be maintained even during standby to extend battery life.

For portable systems, the synchronous buck DC-DC converter is the ideal solution for powering the FPGAs even at lower load currents. But in an ordinary DC-DC converter the efficiency at light loads suffers greatly. This is not important if the load is either "full power" or completely off, since the converter can be disabled. But when powering an FPGA which has power-on standby states, the converter needlessly dissipates power by continuing to switch at the same high frequency required to produce maximum power. In portable systems, it is important to use a converter that transitions to a pulse-skipping or Pulse Frequency Modulation (PFM) scheme.

A typical fixed frequency synchronous step-down converter always runs at a fixed frequency in a continuous conduction mode, whereas a converter in PFM mode transitions to a variable frequency, fixed on-time operation as the load current decreases, and operates in a discontinuous mode to reduce switching losses.

Internal to such a converter is a comparator that samples the output voltage V_O at a fixed frequency f_{PFM} and compares it to a reference voltage V_{REF}. When V_O is less than V_{REF}, the converter generates a fixed on-time pulse through the PWM to charge the output capacitor.

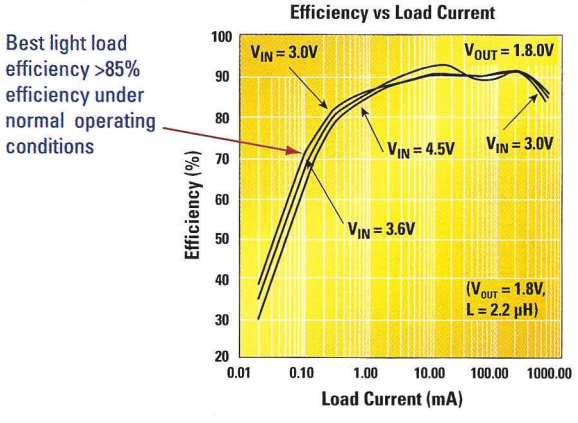


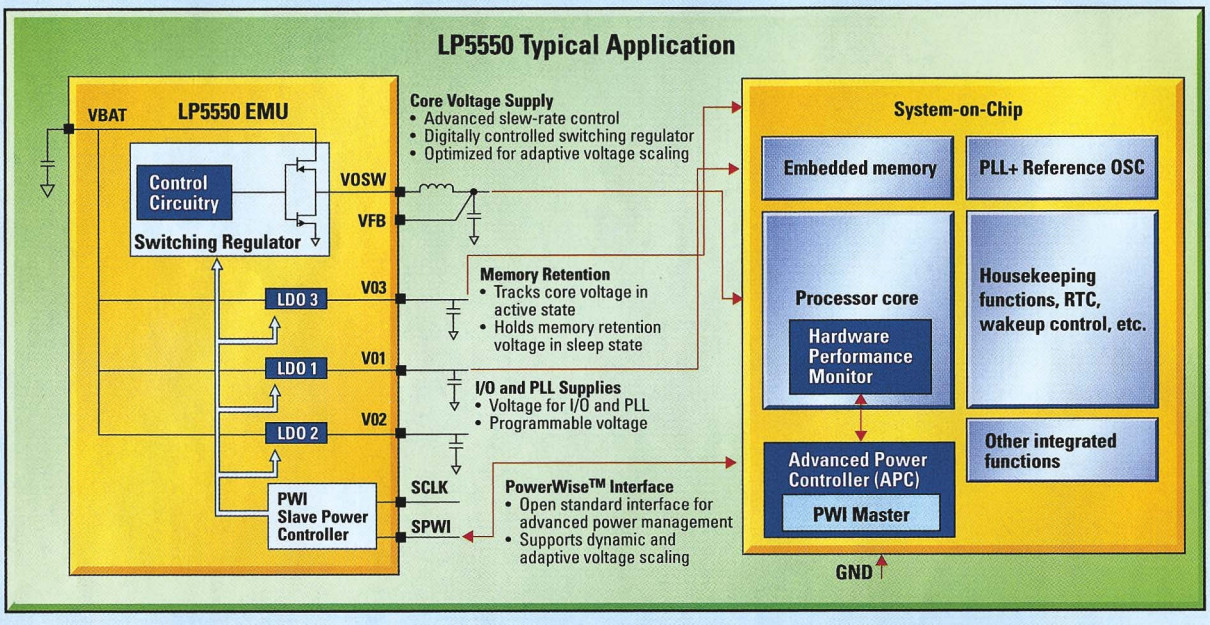
Figure 1. Plot from Device with PFM Shows High Efficiency Across All Loads

PFM operation continues until the output current rises above a certain threshold, at which point normal PWM operation is resumed. There are two main advantages of PFM operation at light loads. One is that the supply current of the DC-DC converter is greatly reduced as much of the internal circuitry is turned off during PFM. Another is that the switching losses of the output stage are minimized because it switches only when required. *(see Figure 1)*

[1] See Power Designer #102 at power.national.com/designer

PWI 1.0-Compliant Energy Management Unit for PowerWise™ Adaptive Voltage Scaling

LP5550 Digitally Controlled PowerWise™ Energy Management Unit for Reducing Processor Power Consumption



LP5550 Features

- High-efficiency PowerWise™ energy management unit (EMU) for adaptive voltage scaling (AVS)
- Compatible with National's PowerWise advanced power controller technology for minimizing processor power consumption
- PWI 1.0 open standard interface compatible
- Reduces power consumption of digital processors by up to 70%
- 3 Programmable LDOs for I/O, PLL, and memory retention supply generation
- Available in an LLP-16 package

AVAILABLE LEAD-FREE

Ideal for use in cellular handsets, handheld radios, cameras, PDAs, battery-powered devices, and portable instruments supplies

Product Highlight:

Digitally-controlled LP5550 reduces power consumption of processors and extends battery life of handheld consumer products

Advanced Topics in Powering FPGAs

The FPGA power designer should choose the power management IC that allows efficient operation in both full load and light load operation. In addition to this, a part with a low quiescent current should be chosen to minimize power loss during standby modes.

Monotonic Rise of Core Voltage

Several FPGAs, ASIC cores, and even processors retain some voltage potential in shutdown. This gives rise to a pre-biased condition where the power converter starts up into this voltage. Pre-biasing can cause initial undesirable changes in the voltage of a converter that is not designed to handle such a load. In particular, it is undesirable for the pre-existing voltage to cause the output voltage of the converter to droop during turn on. The power supply voltage must rise steadily and gradually until eventually stabilizing at its nominal value. This is called a monotonic voltage rise and is necessary for the internal elements in the FPGA to turn on properly. As these elements are turning on during the ramp-up period, the "load" to the power supply will not be constant, so it is important that the converter chosen regulates its output voltage not only during the steady state but also during ramp up. There are two approaches to ensuring a monotonic rise of the voltage.

- One is to increase the bulk capacitance of the converter sufficiently to hold enough charge on the output so that the voltage does not droop during turn on. The additional bulk capacitors in this approach increase both the cost and the footprint.

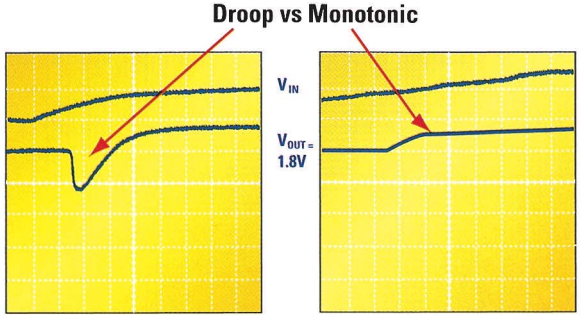


Figure 2.
Comparing Non-Monotonic Rise vs Monotonic Rise

- Another approach is to disable the low-side MOSFET of the synchronous converter and monitor the switching node voltage during the off-time of the high-side MOSFET. The IC remains in pre-biased mode until it detects that the switch node (the point at which the output inductor is connected to the two MOSFETs) stays below 0V during the entire high-side MOSFET's off-time. Once this condition is detected, the low-side MOSFET is allowed to start switching.

Figure 3 shows the switch node as well as the high-side and low-side gate signals during pre-biased startup in a typical synchronous converter. The pre-biased output voltage should not exceed the sum of the supply and gate threshold voltages of the high-side MOSFET to ensure that this device is able to switch during startup.

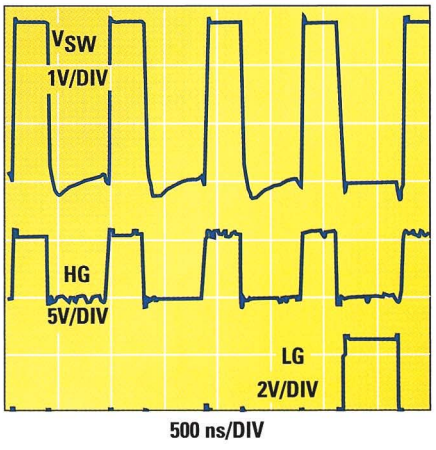


Figure 3.
Switching Waveforms During Monotonic Rise of Outputs

Voltage Scaling to Improve Efficiency

FPGAs are essentially CMOS devices, which scale with advances in process technology. As device geometries scale below 90 nm and operating frequencies increase, both dynamic and static power consumption become more important. Current approaches to FPGA design do not allow for easy reduction of dynamic or static power, although possible theoretically.

SOT-23 Synchronous Constant-on-Time Switching Controller

High-Efficiency LM1770 Synchronous Controller for Low-Voltage DC-DC Conversion

LM1770 Features

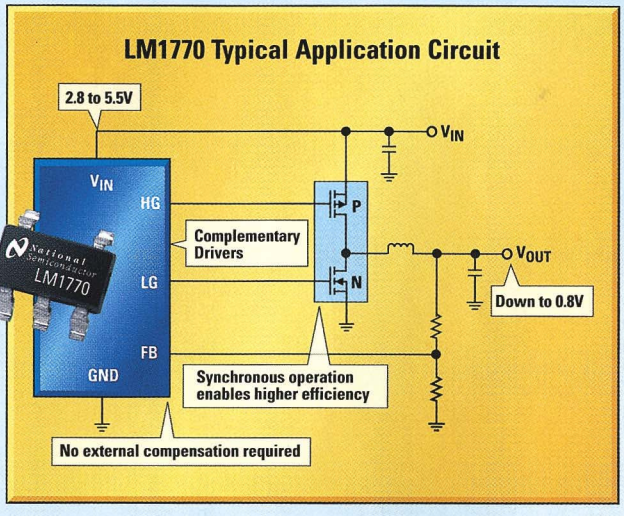
- Adaptive On-Time Control topology requires no compensation components
- Synchronous operation: High-side PFET and low-side NFET enables higher-efficiency and reduced power-dissipation
- Fast-transient response allows for lower values of capacitors
- Low input voltage of 2.8V to 5.5V; Ideal for point-of-load applications
- Three versions of adaptive on-time allows for selection of operating frequency
- Available in SOT23-5 packaging for space-constrained applications

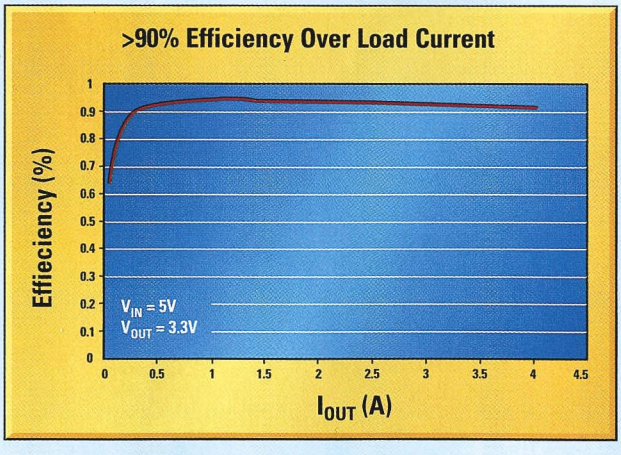
AVAILABLE LEAD-FREE

Ideal for point of load regulation in consumer applications, set-top boxes, cable modems, digital video recorders, printers, servers, and point-of-sale terminals

Product Highlight:

Simplest synchronous controller for up to 5A digital loads





Advanced Topics in Powering FPGAs

Dynamic power can be expressed in terms of switching FPGA activity N, capacitance C, frequency f and supply voltage V_{DD}

$$P_{DYNAMIC} = \frac{1}{2} N.C.f.V_{DD}^2$$

The static or leakage power consumption is due to sub-threshold leakage current I_{sub}, drain-body junction leakage current I_j, and source-body junction leakage current I_b, and is given by

$$P_{STATIC} = V_{DD}I_{sub} + |V_{bs}|(I_j + I_b)$$

where V_{bs} is the body bias voltage.

Manufacturers of portable power systems have realized that the desired small size and long run time requirements of their equipment cannot be met by increasing the energy density of batteries or improving the power delivery efficiency. For such advanced systems, "Dynamic or Adaptive Voltage Scaling" and "Back Biasing" are essential to reduce processor power. The core concept is derived from the equations presented above. The way to reduce dynamic power consumption in a processor is not only to lower the clock frequency as much as possible, but to also reduce the core supply voltage to the minimum value for a given clock frequency. This open-loop technique is called Dynamic Voltage Scaling (DVS). Adaptive Voltage Scaling (AVS) is a closed-loop control technique, which provides substantial improvement to Dynamic Voltage Scaling (DVS). AVS simplifies voltage scaling by inherently compensating for process and temperature variations and eliminating the need for a frequency vs supply voltage table used in DVS. The FPGA or digital processor uses a hardware performance monitor that communicates with the power controller through an open-industry standard PowerWise™ Interface (PWI) and operates at an absolute minimum supply voltage over all operating frequencies. ***Figure 4*** shows an implementation of advanced voltage scaling.

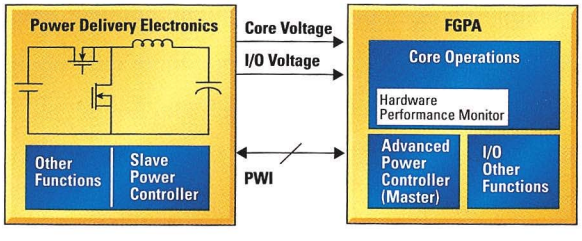


Figure 4. Implementing Advanced Voltage Scaling

Back biasing a circuit such as one in ***Figure 5*** applies -0.8V to -1.5V to the body of the devices, increasing the threshold of the devices and reducing the sub-threshold leakage, thus lowering static power consumption.

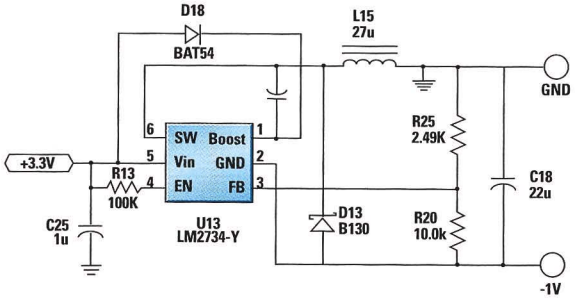


Figure 5. Circuit that Generates a Negative Voltage to Back Bias FPGAs

Conclusion

FPGAs are proliferating rapidly into portable devices. Beyond the basic issues of correctly powering FPGAs, efficiency and battery life also need to be considered. Typically, step-down regulators with provision for high light-load efficiency are best for powering these FPGAs in portable systems. To further improve efficiency significantly, techniques such as adaptive voltage scaling should be implemented. As devices scale downward of 90 nm, managing static power becomes equally important due to the rise in leakage currents in the ICs. The use of innovative back-biasing power management ICs is suggested to reduce sub-threshold leakage and static power. Furthermore, pre-biased loads may exist on the FPGAs during start-up. To ensure monotonic rise of the core voltage is important for their proper functioning, power management ICs that start-up properly into pre-biased loads should be used. ■

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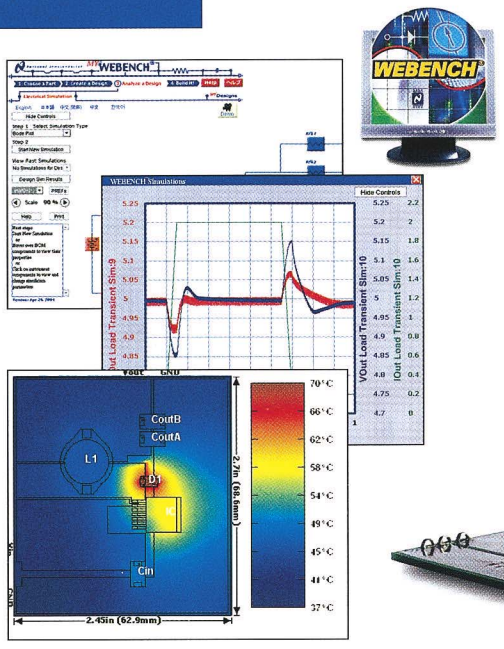
Power Design Tools



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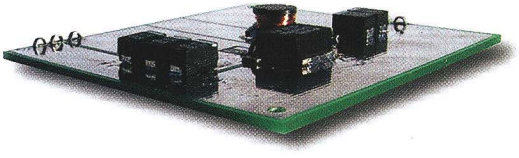

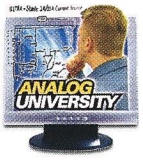

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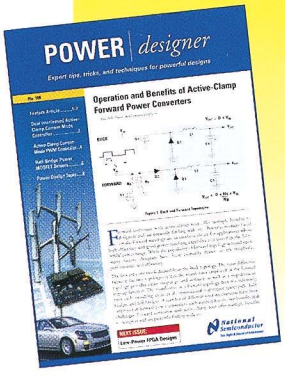

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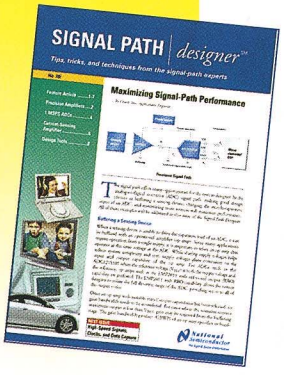

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Going One-on-One

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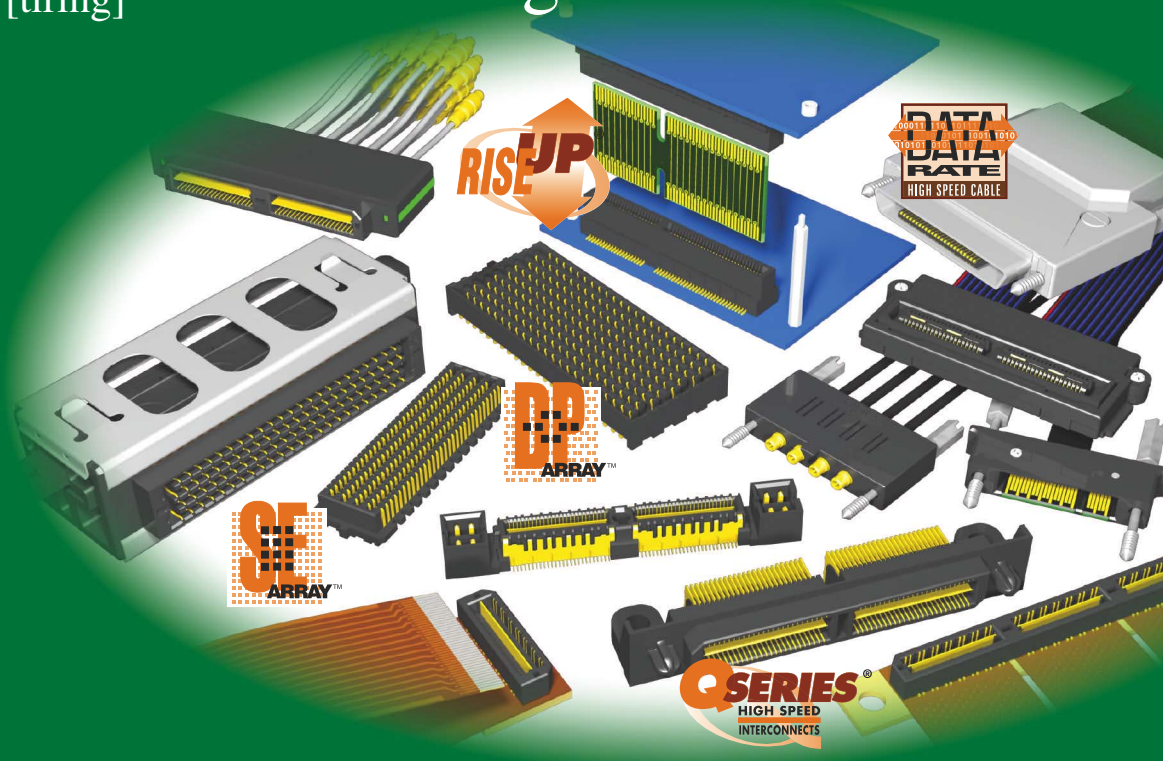
Going Three-to-Three



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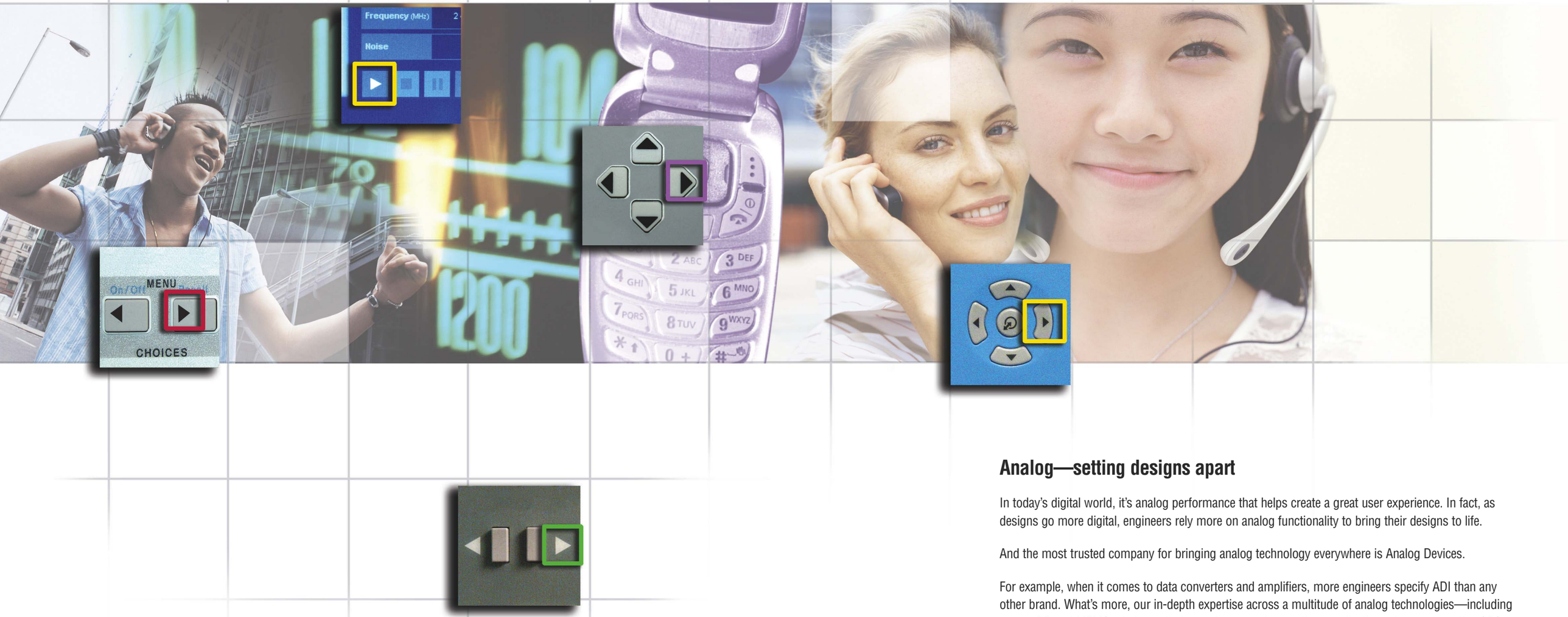

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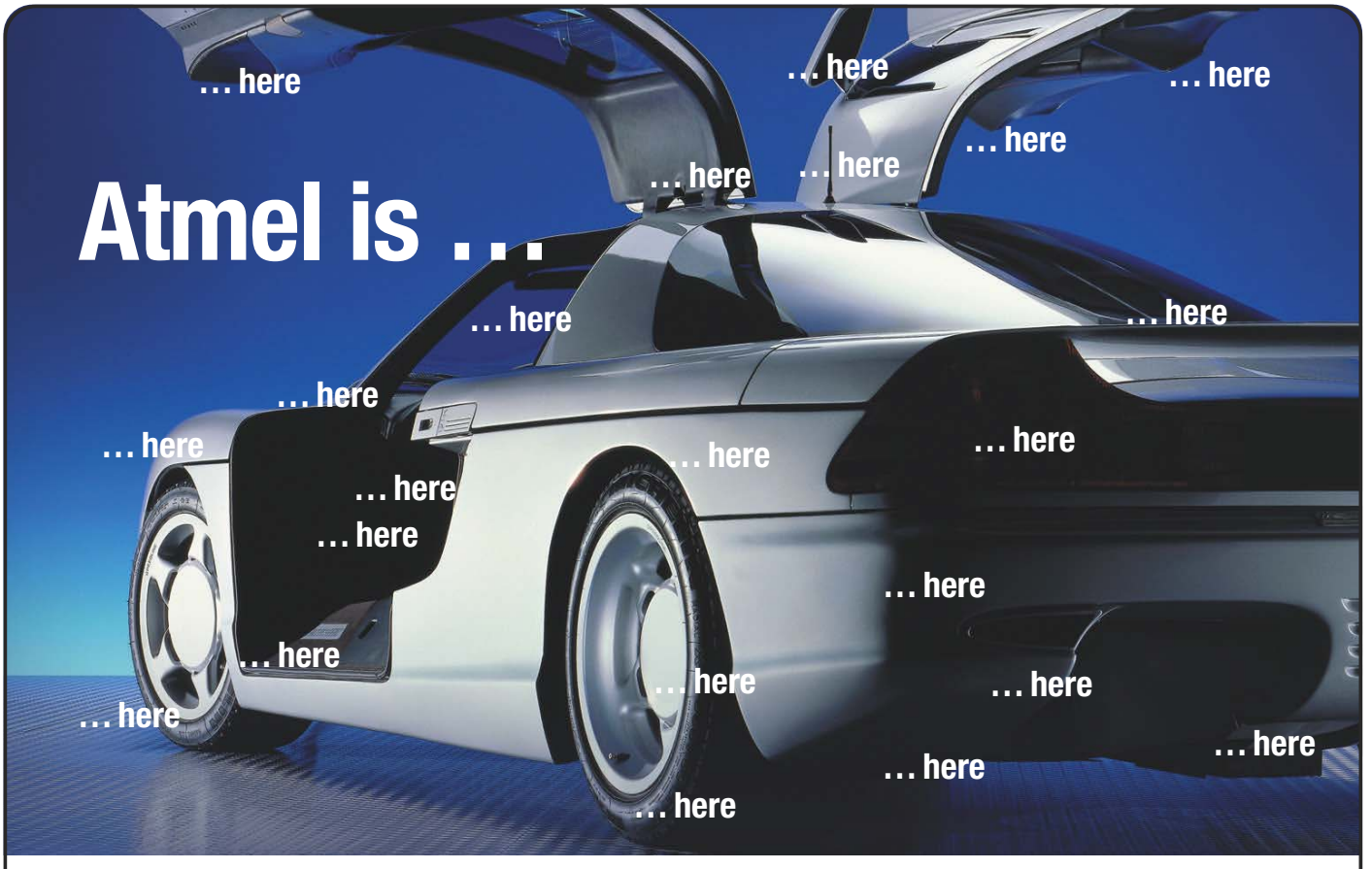

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Popular benchtop-DMM line offers expanded capabilities

Agilent has enlarged its family of DMMs and DVMs. The 34410A, 34411A, and 34405A widen the range of price and performance choices in the company's DMM line, expanding on the popularity of the industry-standard 34401A. The 34410A and 34411A 6.5-digit meters provide greater reading speeds and system throughput, achieving more than 50 times the reading rate of the 34401A.

The 34410A and 34411A, which offer expanded connectivity through USB, LAN, and legacy IEEE 488 ports, comply with LXI (LAN extensions for instrumentation) Class C. The units also offer more measurement functions, expanded measurement ranges, more precise triggering, and as much as 1 Mbyte of reading memory. The 5.5-digit 34405A DMM, says a spokesman, offers a new level of performance in its category as well as PC-standard connectivity.

"The 34401A has been very popular since its introduction in 1991, primarily because of its reliability, ease of use, and exceptional value," says Scott Sampl, vice president and general manager of Agilent's System Products Division. The $1595, 6.5-digit, dual-display 34410A benchtop DMM is compatible with the Agilent Open System framework. The instrument, which is available now, takes 10,000 readings/sec at 5.5-digit resolution and measures dc and ac voltage and current, resistance, capacitance, frequency, and temperature. Accuracy at low and high frequencies is better than that of earlier-generation instruments. The unit has data-logger capability with storage of as many as 50,000 readings, and LAN, USB, and IEEE 488 connectivity.

The 6.5-digit 34411A offers reading rates as great as 50,000/sec at 4.5 digits, 1 Mbyte of reading memory, level triggering, and pretriggering and post-triggering.

The $1995, 6.5-digit, dual-display 34411A benchtop DMM is also available now and is compatible with the Agilent Open System framework. The unit offers better performance than that of the 34410A. Additional features include reading rates as great as 50,000/sec at 4.5 digits, 1 Mbyte of reading memory, level triggering, pretriggering, and post-triggering. A peak-detection feature measures the amplitude of pulses as short as 20 µsec. High acquisition speeds allow the instrument to catch peaks that previous-generation instruments would often miss.

The 5.5-digit, dual-display 34405A benchtop DMM has standard PC-I/O capabilities. It will sell for less than $1000 and should become available in early 2006.**—by Dan Strassberg**

▷**Agilent Technologies**, www.agilent.com/find/34410A and www.agilent.com/find/34411A.

FEEDBACK LOOP

"It isn't only ham-radio operators that suffer: Broadcasters do, too, and, in Europe, are none too pleased with the idea! I'm both a ham and a listener to 'steam' radio and lose out on all counts. What's wrong with ADSL/ADSL2?"

Michael Dixon in *EDN*'s Feedback Loop at www.edn.com/article/CA6280032. Add your comments.

EDA tool adds pc-board-layout, FPGA-design features

Mentor Graphics has bundled some of its PADS and VeriBest pc-board-design software with some of its other legacy pc-board tools and added new team-collaboration software to come up with its new Expedition Enterprise flow. "We've created this core flow to design any pc board," says David Wiens, business-development director for Mentor's pc-board division. "In addition, we integrated many of our tools to create an overall enterprise-design file." Mentor built the Expedition Enterprise flow onto the company's DMS (data-management system) for building and storing library and design data and sharing with large PLM (product-life-cycle-management) tools and thus the rest of the enterprise.

The company has also introduced a constraints-editor system that allows disparate groups to collaborate to create and edit design constraints and come up with BOM (bill-of-materials) costs to share with management and parts-procurement teams. Mentor has also modified several of its design tools, including HyperLynx and ICS (interconnect-synthesis) Pro Explorer for prelayout and signal-integrity analysis, respectively; I/O Designer for FPGA and pc-board integration; DXDesigner for design definition; and PCB Planner for design reuse, variant management, and floorplanning. Wiens says that designers can use third-party tools, but doing so sacrifices a lot of the collaboration abilities Mentor has woven into its product.**—by Michael Santarini**

▶**Mentor Graphics**, www.mentor.com.

12.5-Gbps serial BERT characterizes jitter

Agilent has announced a high-performance serial BERT (bit-error-ratio tester) with jitter-generation capabilities for jitter-tolerance testing of serial devices at speeds to 12.5 Gbps. The N4903A J-BERT provides jitter-tolerance testing for fast, high-quality characterization of next-generation serial devices.

According to Agilent, industry experts expect the next generation of high-speed serial-bus standards with data rates of 5 Gbps and more to emerge by 2006. The increasing speed will cause significant signal-integrity and jitter issues during the design and test of new serial-bus devices. In addition, new transmission techniques, such as spread-spectrum clocking, will make characterizing device performance more difficult and time-consuming.

The N4903A complies with the latest serial-bus standards and provides calibrated jitter-composition measurement and automated jitter characterization in a single box. The unit provides complete calibrated jitter-composition measurement for stressed-eye testing of receivers. Automated and compliant jitter-tolerance testing covers popular serial-bus standards, such as PCI Express, SATA (serial advanced-technology attachment), Fibre Channel, FB-DIMM (fully buffered dual-in-line-memory module), CEI (common electrical interface), Gigabit Ethernet, and XFP (10-Gbps small-form-factor pluggable module).

"Jitter-tolerance testing is the most complex and time-consuming measurement that design teams of next-generation serial devices have to deal with," says Siegfried Gross, vice president and general manager of Agilent's Digital Verification Solutions Division. Agilent spokesmen claim that the unit is the first and only complete, one-box jitter-tolerance tester.

The N4903A J-BERT can completely, automatically, and quantitatively characterize jitter in serial-data streams to 12.5 Gbps.

The Agilent N4903A high-performance serial BERT includes built-in, automated, calibrated, and compliant jitter-tolerance testing with sources of intersymbol and sinusoidal interference, as well as periodic, random, and bounded, uncorrelated jitter. These capabilities enable fast, precise stressed-eye testing with more than 50% eye closure.

The instrument fully supports serial buses' complex data patterns. With the bit-recovery mode, it can analyze unpredictable traffic, enabling more realistic test scenarios. A new pattern sequencer speeds test development by simplifying the setup of complex training sequences. Other features include built-in clock-data recovery; new subrate-clock outputs; spread-spectrum clocking, which significantly simplifies the clock setup; and accurate characterization with the cleanest eyes, 20-psec transition times, and 50-mV analyzer sensitivity. Prices start at $120,000 for the 7-Gbps version and $160,000 for the 12.5-Gbps version.**—by Dan Strassberg**

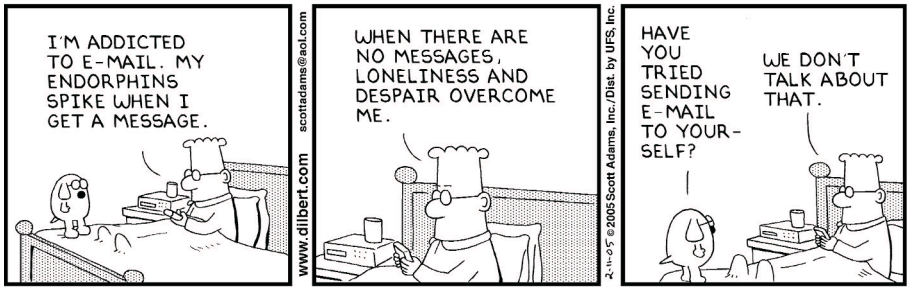
▷**Agilent Technologies**, www.agilent.com/find/n4903.

FEEDBACK LOOP

"Another 'dirty old man' of electronics, dithering does not reduce the impact of interference to many users of the spectrum. It worsens it for many. The local noise floor had risen by 20 dB in recent years, mainly due to incompetently 'designed' power supplies in TVs and other domestic units."

Alan Melia in *EDN*'s Feedback Loop at www.edn.com/article/CA6262536. Add your comments.

DILBERT *By Scott Adams*



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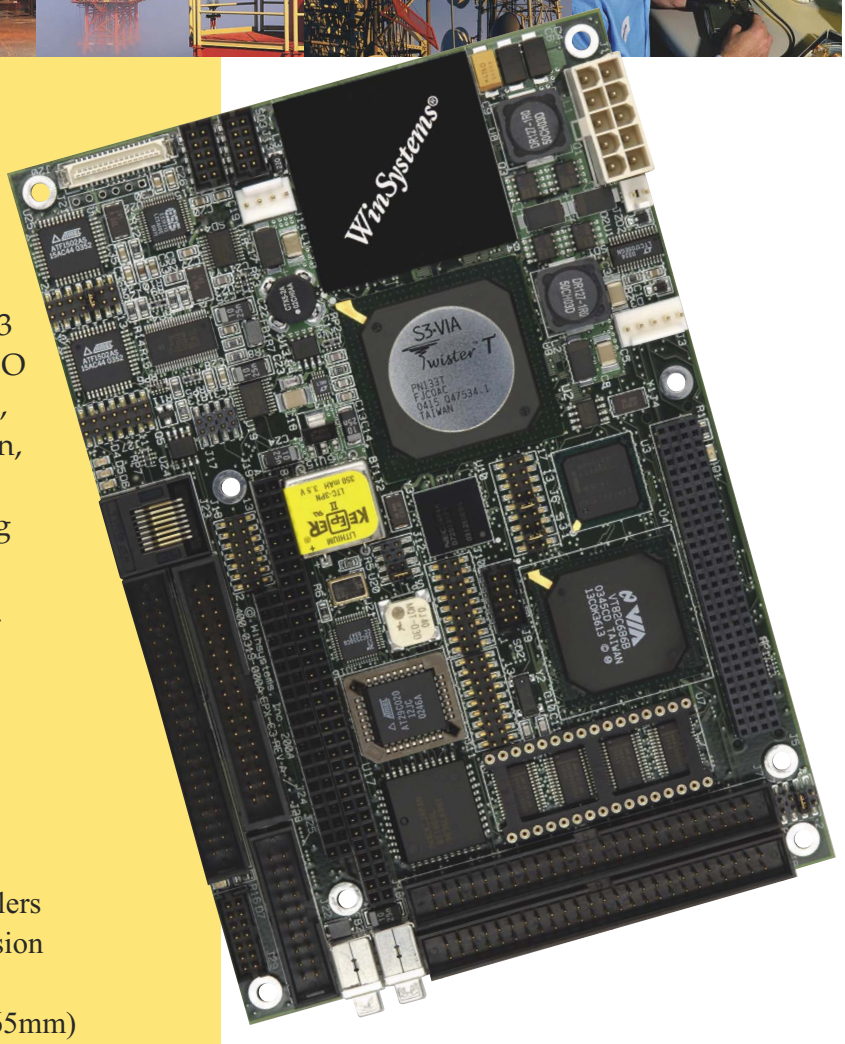

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FPGA physical-synthesis tool knows the fastest routes

Synplicity boasts that its new graph-based FPGA physical-synthesis tool uses inside knowledge of FPGA architectures to deliver a 5 to 20% performance improvement over the company's popular logic-synthesis tool. In addition, the company claims, 90% of all routed nets fall within 10% of final timing correlation. The new tool, Synplify Premier, will replace the company's Amplify physical-synthesis tool and become Synplicity's top-of-the-line FPGA-synthesis tool.

The key to the tool's performance boost is its graph-based physical-synthesis engine, says Jeff Garrison, the company's director of FPGA-product marketing. Because FPGAs are prerouted, they limit the paths you can take between two functions. Synplicity has turned that architectural shortcoming into a design advantage by doing detailed analyses of the interconnect within certain FPGA families, Garrison says. Synplify Premier's graph-based engine has access to that information, which it uses to accurately find the fastest route to interconnecting blocks within the FPGA.

Most FPGA physical-synthesis routers use proximity-based techniques originally designed for ASICs. Proximity-based routers attempt to place functions next to or close to each other to reduce the length of the interconnect. "But, in an FPGA, placing one function right next to another function may not be the fastest route between the two functions," Garrison says. "It's like commuting to work: You sometimes drive a bit out of the way to get to work faster."

In addition, users of Synplify Premier need not synthesize and floorplan their designs if their designs consist entirely of synthesizable RTL code. Users can feed the tool RTL code, push a button, and watch the tool find the optimum floorplan, placement, and routing. The tool concurrently performs synthesis, floorplanning, placement, and prerouting, and the vendor's proprietary router performs detailed routing. However, designers who are using a hard or a firm macro or who want to tweak the layout must buy the DesignPlanner floorplanning add-on, which costs $15,000 to $29,000 more than the $34,000 to $74,000 cost of Synplify Premier.

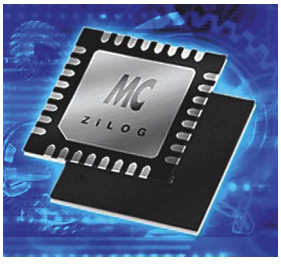
The top-of-the-line version of Premier also features a built-in version of Synplicity's Identify debugging engine and a scaled-down version of the company's Certify ASIC-prototyping tool. The scaled-down prototyping technology allows users to create ASIC prototypes on a single FPGA. This creation includes most FPGA-prototyping projects, according to Garrison, because many users employ a single FPGA to test new functions they plan to add to a design previously implemented in an ASIC. Users will need full-blown Certify if they want to prototype ASIC designs in more than one FPGA.

—by Michael Santarini

▷**Synplicity**, www.synplicity.com.

Flash, 8-bit processor targets motor control

Zilog's Z8 Encore! MC family of 20-MHz, 8-bit flash microcontrollers targets sensorless BLDC (brushless-dc) and ac-induction motor-control applications. The eight-channel, 10-bit ADC samples in 2.5 µsec and can couple a time-stamp feature with the three-phase, six-channel, 12-bit PWM-output module to enable accurate speed control. Another feature is direct routing of the current-sensing module to the PWM module to enable fast shutdown of the system during an overcurrent fault. The first three devices in this series, the Z8FMC04100, Z8FMC08100, and Z8FMC16100, each offer 512 bytes of RAM with 4 to 16 kbytes of on-chip flash memory.



The MC family of 20-MHz, 8-bit flash microcontrollers targets motor-control applications.

The 5×5-mm, 32-pin QFN package integrates an operational amplifier; an analog comparator; and a 2%-accurate, 5.53-MHz internal oscillator in packages that support standard 0 to 70°C and extended −40 to +105°C temperature ranges. These devices are available now as standard-temperature devices for $2.26 to $2.50 (5000). Zilog offers internal factory programming for these devices. Third-party programming support includes BP Microsystems (www.bpmicro.com), Hi-Lo Systems (www.hilosystems.com.tw), and Data I/O (www.dataio.com). Zilog's motor-control-specific development-tool suite retails for $199.95, and it includes a BLDC motor, an application board, ZDS II with a full ANSI C compiler, motor-control software code, and an optoisolated USB smart cable for debugging and programming. A $1999 in-circuit-emulator kit includes package adapters and event-trace functions.

—by Robert Cravotta

▷**Zilog**, www.zilog.com.

FEEDBACK LOOP

"It is hard to believe that, in this technological world, we are considering such a 'Stone Age' solution. The radio spectrum is part of the environment and, as such, is a limited resource. Once it is rendered unusable, it will be, like the rain forest, very difficult to recover."

Alan Melia in *EDN*'s Feedback Loop at www.edn.com/article/CA6280032.

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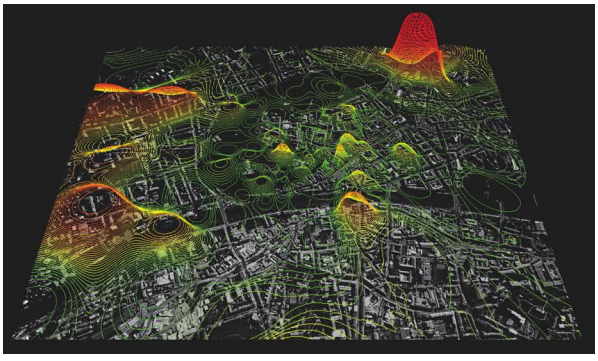


RESEARCH UPDATE

BY MATTHEW MILLER

Electronic maps track cell-phone use

Researchers at the Massachusetts Institute of Technology's Mobile Landscapes project have mapped the city of Graz, Austria, in real time by monitoring the usage of tens of thousands of cell phones. The researchers obtained anonymous cell-phone data from the leading cell-phone operator in Austria, A1/Mobilkom (www.a1.net), to develop the project. The technology creates electronic maps of cell-phone use in the metropolitan area of Graz, Austria's second-largest city.

To obtain the maps, researchers used the density, origins, and destinations of cell-phone calls and the position of users they tracked at regular intervals. They used this data to create computer-generated images that they then overlay with one another and with geographic and street maps of a city to show the peaks and valleys of the landscape, as well as the peaks in cell-phone use (photo). Locating and tracking mobile devices target use in law enforcement and urban planning. "This technology opens up new possibilities for urban studies and planning," says Carlo Ratti, an architect and engineer at MIT. "The real-time city is now real: a system that can continuously sense its condition and can quickly react." To learn more, go to http://web.mit.edu/newsoffice/2005/cellphones.html. For real-time images of Graz, go to http://senseable.mit.edu/projects/graz/graz.htm.

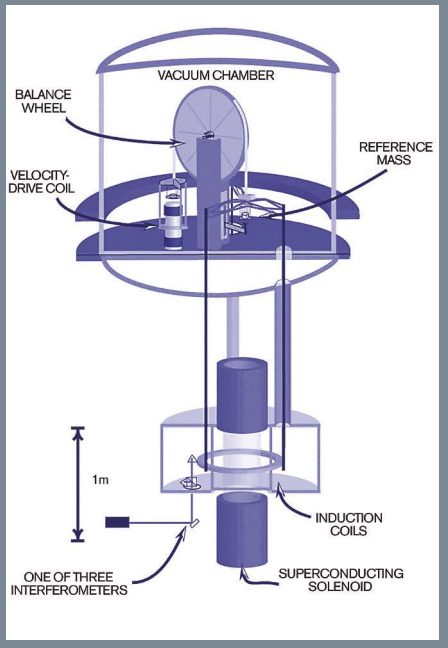
▷**Massachusetts Institute of Technology**, www.mit.edu.

Ethernet-over-optical transmission achieves 100 Gbps

Lucent Technologies has announced the first transmissions of 100-Gbps Ethernet-over-optical technology. A research team at the company delivered a 107-Gbps optical-data stream, representing 100-Gbps data transmission and a 7% overhead for error correction. The technique uses duobinary signaling and a single-chip optical equalizer. Duobinary signaling uses positive, negative, and zero signal levels to represent a binary signal for communications transmission. The signals require less bandwidth than traditional NRZ (non-return-to-zero) signals. The optical equalizer, which Bell Labs invented two years ago, compensates for almost all intersymbol interference arising from modulator-bandwidth limitations in an optical, 107-Gbps, NRZ, electronic-time-division-multiplexing transmitter.

▶**Lucent Technologies**, www.lucent.com.

Watt-balance method accurately defines the kilogram



Researchers at the National Institute of Standards and Technology have spent years conducting experiments to find a reliable definition based in nature to replace the current international standard for the kilogram, a century-old cylinder of platinum-indium alloy about the size of a plum. Now, they have achieved that goal, using a watt-balance method they first tried in 1998. This time, they received the same results as with earlier experiments but with better accuracy, thanks to improved hardware.

The watt balance is a two-story-high apparatus that redefines mass in terms of fundamental physics and quantum standards. It measures the force necessary to balance a 1-kg-mass artifact against the pull of the Earth's gravity, as well as two electrical values (photo). The watt balance is one of two leading approaches for redefining the kilogram. The other approach counts how many atoms of a specific atomic mass equal the mass of 1 kg. The latest NIST measurements have an uncertainty of 0.052 ppm compared with 0.087 ppm in the 1998 experiments. These measurements are more precise than any previous results by any research group using either approach.

For additional background on efforts to redefine the kilogram in terms of natural properties, see www.nist.gov/public_affairs/newsfromnist_redef_kilogram.htm.

▶**National Institute of Standards and Technology**, www.nist.gov.

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Lithium ion gets a recharge

The fuel cell—a cigarette-lighter-sized power source that you can refill—is one way to solve the problem of using heavy and short-lived batteries. That's the message Intel sent in its August announcement of a tie-in with Matsushita Battery Industrial Co Ltd to develop an eight-hour, "all-day" laptop battery. The two big guns will focus on lithium-ion-battery technology. That's good news for systems designers, who won't have to fundamentally change their design methods for portable devices. "With lithium ion, there are still some tricks that can make them last longer," says Sara Bradford, research manager for power supplies and batteries at Frost & Sullivan (www.frost.com).

Lithium ion has become the battery technology of choice for laptops and cell phones, which tend to drive power-source developments in consumer devices. Lithium-ion-based batteries accounted for 71% of rechargeable batteries in 2001, which the research company expects to rise to 79% by 2010.

The Intel-Matsushita effort will drive key Japanese battery makers to more quickly reach milestones in their technology road maps, according to Robin Sarah Tichy, product-marketing engineer at Micro Power Electronics Inc, a supplier of systems for batteries. "We see an increase in capacity for lithium ion, which won't change anything from a design point of view," Tichy says. "The voltage should stay approximately the same."

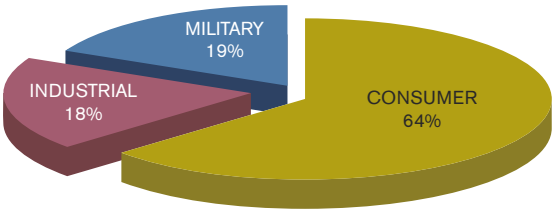
But, inevitably, handheld-equipment designers will face challenges from fuel cells, which should gain some traction by the end of the decade, according to Bradford. Laptops are expected to adopt fuel cells first, but the smaller device platform of cell phones creates a tougher design challenge. Fuel cells got a boost in 2004 when mobile-phone giant Nokia Corp (www.nokia.com) announced development strides and predicted wide use by 2006. In March, however, Nokia scaled back development work because it couldn't find a reliable supply of methanol, which the company used in its product.

Fuel cells face other hurdles, Bradford says. No one knows how to best integrate them: as clip-on or as stand-alone devices. Moreover, standards and regulatory issues remain. Fuel cells contain flammable liquids, which the Federal Aviation Administration prohibits from airplanes until 2007.

Bradford believes fuel cells won't eliminate batteries but will appear in combination with them, serving as rechargers, eliminating the need to plug a cord into a wall. Breakthroughs, however, could turn fuel cells into a disruptive technology. Every gadget manufacturer is seeking a big battery-life increase for sharp competitive advantage, and Motorola (www.motorola.com), Toshiba (www.toshiba.com), and NEC (www.nec.com) are among the players pouring resources into fuel-cell developments for cell phones and laptops.

—by Drew Wilson

▷**Matsushita Battery Industrial Co Ltd**, www.panasonic.co.jp/mbi/.
▷**Intel**, www.intel.com.
▷**Micro Power Electronics**, www.micro-power.com.



The market for fuel cells should grow to 125.2 million units by 2010, according to Frost & Sullivan.

For more on battery technologies, see this issue's cover story on pg 58.

IDEs enhance automotive-design productivity

12.05.05

To handle the complex development, testing, and integration of microprocessor-driven vehicle functions, design engineers are opting to use tools that offer IDEs (integrated development environments). According to a CG-Smith Software spokesman, IDEs for developing software for microcontrollers must support CAN (controller-area-network), LIN (local-interconnect network), MOST (mobile-open-systems-technology), and other automotive protocols. They must also incorporate the code-optimization techniques for memory-constrained designs. CG-Smith uses commercial compilers and debuggers from Lauterbach (www.lauterbach.com), IAR (www.iar.com), Noral (www.noral.com), and Green Hills (www.ghs.cm).

Sridhar Perepa, technical director at MindTree Consulting, deploys Wind River Systems' (www.windriver.com) VX Works, Texas Instruments' (www.ti.com) Code Composer, and other processor-specific development tools from Atmel (www.atmel.com) and Infineon (www.infineon.com) for automotive-electronics designs. According to S Renukaprasad, general manager of automotive electronics at Wipro Technologies, the IDEs in the company's development centers include Freescale (www.freescale.com) and MetroWerks (www.metrowerks.com) compilers, QNX's (www.openqnx.com) Momentics, Microchip Technology's (www.microchip.com) MPLab, and NEC's (www.nec.com) PM Plus to support designs for entertainment applications, keyless-entry systems, and electronics modules.

Meanwhile, KPIT Cummins is developing the Corona IDE for automotive and industrial applications. The company developed the Eclipse-framework-compliant, Windows-based IDE using C, C++, and assembly language.**—by Chitra Giridhar, *EDN Asia***

▶**CG-Smith**, www.cg-smith.com.
▶**Mindtree Consulting**, www.mindtree.com.
▶**Wipro Technologies**, www.wipro.com.
▶**KPIT Cummins**, www.kpitcummins.com.

Blackfin is action packed

▶ V300 Portable Media Player

Open Source
Car Telematics
IP TV
Mobile TV
Telepresence
Biometrics
Driver Assistance
▶ **Streaming Media**
High Definition
Effects Processing
Triple Play
Image Processing
VoIP
Embedded Security
GSM/EDGE
Baseband Processing
Digital Radio
Global Positioning
Packet Processing
GCC/Linux
Cryptography
Rights Management

Low power, riveting performance

The V300 Portable Media Player needed a processor that could enable 8 hours of MPEG-4 or MJPEG video playback and 16 hours of MP3 music, and run its operating system and application set. After auditioning a long list of prospects, Blackfin® got the role. Why? Blackfin easily met the V300's performance goals while powering the system from a 600 mAh battery. Then Blackfin nailed the part with $5 to 1200 GMACS scalable performance for content and applications.

Get started using Blackfin now:
analog.com/blackfin-is-everywhere

ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Quality factor

What matters most in a capacitor depends entirely on how you use it. For example, capacitors in the Electra pulsed-power fusion-ignition system require a voltage rating of at least 5 million volts, with an incredible energy-storage density. Solution? Build a massive coaxial structure and fill it with water (**Reference 1**).

A 1V switching power supply has vastly different requirements. This design needs capacitors with low ESR (equivalent series resistance). Switching power designs surge huge currents through the capacitors, back and forth, constantly charging them up and down. Even a tiny amount of series resistance in the presence of all that surging current can overheat, possibly bursting the package and spilling dielectric goo all over your board. I have been around systems that actually erupt in flames when that happens. To reduce the ESR at switching-power-supply frequencies, thick copper plates, firmly bonded to the lead frame, really help.

Capacitors in narrowband filters need a high Q, or quality factor. This number, which is closely associated with the dissipation factor, determines how long a resonant circuit will ring. To make highly resonant, ringy circuits, you need high Q. Low-noise oscillators, IF filters, and many other circuits need high-Q capacitors. To make a high-Q capacitor at microwave frequencies, you reduce the skin-effect resistance of the leads and plates using silver-plated construction and specify an expensive, low-loss dielectric.

Specifications having to do with initial tolerance, temperature drift, and long-term stability govern the inherent accuracy of your circuits. These specifications require stable, accurately machined dielectric materials. Properly aged, low-dielectric-constant ceramic materials fit this bill.

Ordinary, garden-variety, low-Q capacitors will work better in your digital application.

If you need a specific, well-known value of temperature coefficient to compensate for a problematic temperature drift in another part of your circuit, other dielectric materials are available to do that job. Imagine how low the volumes must be (and how high the prices) on these types of specific parts!

Now comes the application I care most about: bypass capacitors for high-speed digital products. Depending on your power-system architecture, these bypass capacitors must cover a range of frequencies—from a few megahertz to several hundred megahertz, providing a low-impedance connection between power and ground all across that band. For that purpose, pick the smallest package (smallest inductance) your manufacturing people will let you use, and in that package size choose the largest value of capacitance you can reliably purchase from multiple vendors.

For this application, you do not need high voltage, low ESR, high Q, or great stability. Ignore those parameters. Especially, do not pay extra money for "microwave-grade" high-Q capacitors; ordinary, garden-variety, low-Q capacitors will work better in your digital application. High-Q capacitors exacerbate resonances in a circuit, and resonance is the last thing you need in a power-distribution system. Digital folks want low-Q capacitors.

Taking the "low-Q" insight one step further, it would be great if you could purchase capacitors that *guarantee* a low quality factor (a *minimum* value of ESR). To help make that situation possible, well-respected power-system designer Istvan Novak will lead a TecForm discussion at DesignCon 2006 in Santa Clara, CA, looking into ways of making low-Q, high-ESR capacitors. I wish him the best of luck at that session, as low-Q construction is something from which we all could benefit. EDN

REFERENCE

1 www.ge-prize.com/Laureates/jan/lecture/.

MORE AT EDN.COM

Go to www.edn.com/051205hj and click on Feedback Loop to post a comment on this column.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

Blackfin is picture perfect

▶ Leica Digital-Modul-R digital back for analog SLR cameras

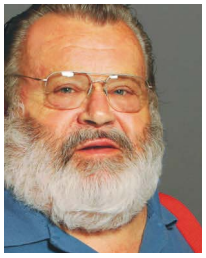
- Telepresence
- Biometrics
- Driver Assistance
- Streaming Media
- High Definition
- Effects Processing
- Triple Play
- ▶ **Image Processing**
- VoIP
- Embedded Security
- GSM/EDGE
- Baseband Processing
- Digital Radio
- Global Positioning
- Packet Processing
- GCC/Linux
- Cryptography
- Rights Management
- Open Source
- Car Telematics
- IP TV
- Mobile TV

10 megapixel image compression in ½ second

To equip professionals with a powerful and compact photography module for its analog SLR cameras, Leica Camera AG needed a small high performance processor. So the company focused on Blackfin's advantages. These included dual-processing cores up to 600 MHz that use just 144 mm^2 of board space, and Blackfin's ability to do Leica's color interpolation, auto exposure, auto white balance, gamma correction, and JPEG compression of 10 megapixel images. Smaller footprint, higher performance: No wonder Blackfin® is everywhere.

Get started using Blackfin now:
analog.com/blackfin-is-everywhere

ANALOG DEVICES



BY RON MANCINI

Anatomy of a current-feedback op amp

A previous column dealt with the VFOA (voltage-feedback op amp, **Reference 1**). This column explains the CFOA (current-feedback op amp) and includes a performance analysis.

Slew rate and frequency performance are the CFOA's strong points, but its precision and CMRR (common-mode-rejection ratio) are subpar to those of a VFOA's. **Figure 1** shows a CFOA, and circuit analysis explains these conclusions.

The V_P input has a high impedance because it connects to the input of a voltage buffer. The V_N input has a low impedance because it connects to the output of the same buffer. One immediately obvious difference between a CFOA and a VFOA is that the VFOA has matched high-input impedance, and the CFOA's input impedances differ in value. Input-stage precision requires matching, and the CFOA requires that the manufacturer match two NPN and two PNP transistors operating at different current levels. Normally, there is no way to match the input and the output stage of a buffer; thus, you don't gain precision from matching. Furthermore, few high-frequency-amplifier designs require high precision, because the signals are ac-coupled or small, or they contain no information in the dc content. This amplifier has transimpedance resulting from the current mirror rather than gain, like the VFOA. The transimpedance performs the same function as gain; hence, the precision must come from dividing the transimpedance into the error term. And, although that step can result in millivolt input-offset voltages, it seldom achieves microvolt input-offset voltages.

The most common operating mode for a CFOA is as a noninverting amplifier, because the inverting input impedance is low. You can use the CFOA as a differential amplifier, but this mode yields poor CMRR, because the input-voltage offset and input impedances do not match well. The CFOA yields poor precision and poor CMRR; thus, it finds use in applications that don't require these characteristics.

The CFOA is essentially two current buffers separated by a current mirror. Current buffers are fast, and current mirrors are reasonably fast, so the CFOA is a high-speed device with high gain bandwidth. The slew rate is not internally limited in a CFOA, because the current available to charge C_C is not limited. When the input-voltage swing is large, it forces large currents into the current mirrors, and an increasing portion of the mirror current is available to enhance the slew rate. An additional feature that enhances slew rate is the input current that can flow from the V_N input, through the feedback resistor, and into the load. The input buffer is fast, so the feedback current is almost instantaneous, causing an initial high slew rate. **Table 1** summarizes the final comparison. EDN

TABLE 1 COMPARISON OF VFOAs AND CFOAs

Parameter	VFOA	CFOA
Input impedance	Matched, high	Mismatched
Precision	Very high	Medium
CMR	Very high	Medium
Bandwidth	Medium high	Very high
Slew rate	Medium	Very high
AC error	Medium	Low

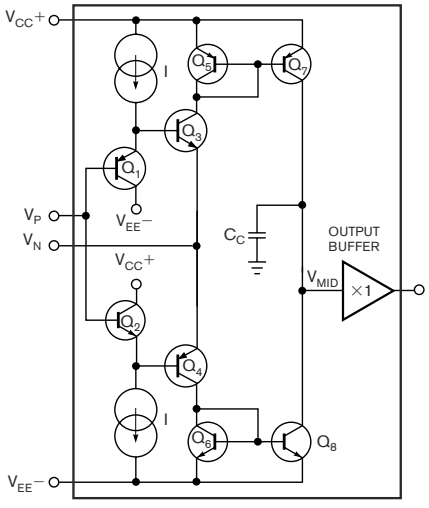


Figure 1 Connecting the CFOA inputs to a buffer input/output precludes precision.

REFERENCE

1 Mancini, Ron, "Anatomy of a voltage-feedback op amp," *EDN*, Oct 27, 2005, pg 40, www.edn.com/article/CA6275426.

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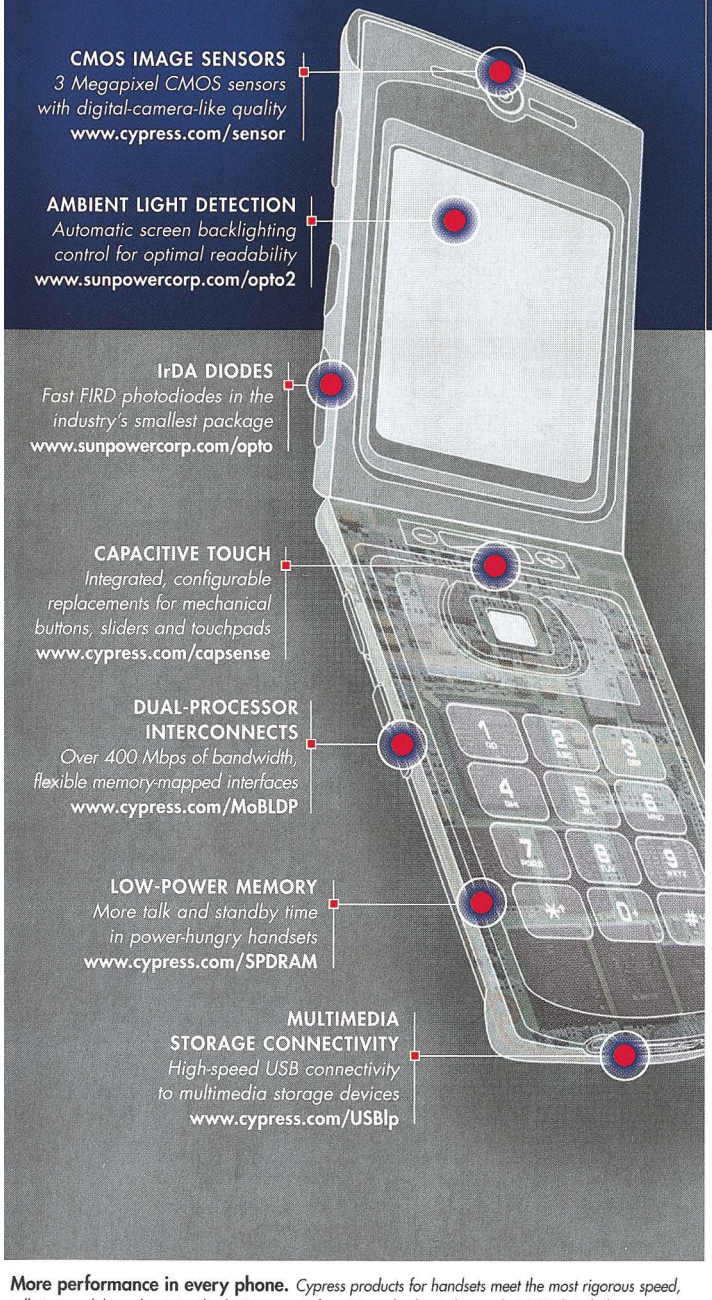
Go to www.edn.com/051205rm and click on Feedback Loop to post a comment on this column.

NOTE FROM THE AUTHOR

I am retiring from Texas Instruments after a prosperous, interesting, and rewarding career. This is my last regular column for EDN. *I wish you all well; I hope you have enjoyed reading these columns as much as I have enjoyed writing them.*

Cypress Handset Solutions



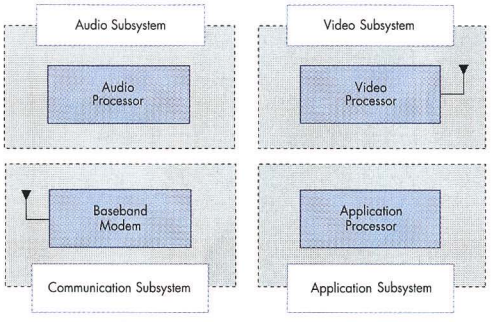
More performance in every phone. *Cypress products for handsets meet the most rigorous speed, talk time and throughput standards. For more information, check out the product URLs listed above.*

Maximizing data transfer in modular handset designs.

by Hervé Letourneur, Product Manager, Cypress Semiconductor Corp.

The convergence of functions in the mobile handset is creating new challenges. The article below explores flexible, modular handset platforms that can be upgraded with minimal redesign. For other handset-related material — including application notes, reference designs and articles on capacitive sensing and interprocessor connectivity — please visit Cypress's Handset Solutions Center at ***www.cypress.com/handsets****.*

In addition to basic voice functionality, today's mobile phone offers camera functions, video, games, 802.11 connectivity, MP3 players, and computer synchronization. A flexible architecture includes multiple subsystems that can be upgraded independently with minimum impact on the other blocks.



Example of a modular architecture with 4 subsystems

The figure above shows an example of an architecture using four subsystems. One is dedicated to communication and is centered around a baseband modem. Another is dedicated to applications, perhaps an application processor running 3D games. A third block could provide connectivity to video broadcast (DMB or DV-H), and a fourth could support MP3 player functions.

These subsystems can be used to build specific platforms and need not be altered when other blocks are changed. An entry-level platform would probably use only one of these blocks, while a more advanced platform could use up to four, depending on the target market.

In a modular architecture, each block can be upgraded independently. For instance, the communication block can be upgraded to

CYPRESS
PERFORM

CYPRESS PRODUCT	OVERVIEW	FEATURES
CMOS IMAGE SENSORS	As camera phones migrate to higher resolutions, Cypress is ready with high-performance 3- and 1.3-megapixel image sensors that offer scalable upgrade paths from lower resolutions. Cypress's image sensors have superior low-light sensitivity, better signal-to-noise ratio, and the widest dynamic range in the industry. They output a RAW Bayer pattern, enabling easy connections to most multimedia processors and analog binning that delivers true VGA video. Cypress sensors don't require microlenses, and still produce greater than 70 percent fill factor.	**3 Megapixel** ■ 1/3" optical format ■ Analog binning – horizontal and vertical ■ Increased SNR ■ 72dB dynamic range ■ Ease of manufacturing
DUAL-PROCESSOR INTERCONNECTS	Today's high-performance mobile phones use a multi-processor or modular architecture to deliver advanced multimedia applications. Cypress's MoBL® dual-ports offer the most flexible way to connect two processors (typically baseband modem and application processor). The dual-ports enable high-throughput data transfer required for 3G and allow devices with different I/O line voltage levels or frequencies to connect. By using a standard memory interface for data transfer, they enable communication and application subsystems to evolve independently, with no constraints from proprietary protocols.	**Flexible Interconnect** ■ Most flexible interconnect, using universal SRAM memory bus ■ High bandwidth, with more than 400 Mbps available ■ Allow different voltage, frequency and width on each port ■ Enable modular architectures with independent subsystems
CAPACITIVE TOUCH	Capacitive sensing is an elegant, cost-effective replacement for buttons and switches in mobile phones. Using no moving parts, capacitive sensing increases durability and effective lifespan of personal electronics with no added cost. PSoC™ CapSense™ technology brings a flexible architecture, system integration capabilities, and cost reduction potential to interface applications. It offers the ability to implement multiple capacitive sensing elements in a single device. Award-winning design tools accelerate design effort and decrease time-to-market while bringing differentiation, fashion and functionality.	**Functionality** ■ Buttons ■ Sliders ■ Touchpads ■ Touch wake-up **Configurable** ■ Adapt to design changes ■ Move across platforms ■ Small packages
LOW-POWER MEMORY	Cypress has shipped more than 400 million units in handheld applications. We provide low-power, high-bandwidth, low-cost solutions to meet the performance requirements of battery-powered applications. **Portfolio Highlights:** ■ Pseudo-Static RAM (PSRAM)/CellularRAM™ offering high bandwidth and low standby current ■ MoBL® SRAM with ultra-low standby current	**CellularRAM™ 1.5** ■ DRAM core with SRAM interface ■ Backward-compatible to standard SRAM ■ Async/Page mode ■ NOR Flash burst mode (sync burst read/async write) ■ Sync burst read and write mode up to 104 MHz
MULTIMEDIA STORAGE CONNECTIVITY	Today's mobile phones include advanced features such as the ability to record video, play music, and send multimedia messages. Manufacturers are requiring both PC connectivity via USB and increased internal storage for various types of multimedia files (MP3, MP4 and JPEG). Designed with I/O controller capability for high-speed USB 2.0 connectivity, storage devices (NAND Flash, HDD), and application processors, the Cypress High-Speed USB LP family enables both PC connectivity and mass storage capability for the mobile phone in a small package with low power.	**Flexible I/O Control** ■ High-speed USB 2.0 connectivity ■ 8-/16-bit programmable interface for application processor ■ Storage interface (ATA/ATAPI, Flash) **HDD and Flash Storage Support** ■ Compatibility to industry HDDs and NAND Flash ■ Increase read/write to HDD using UDMA ■ Flash read up to 15 Mbps, write up to 11.7 Mbps

1.3 Megapixel

- ¼" optical format
- No microlenses
- SOC version includes
  - Auto white balance
  - Camera control I2C
  - Color correction
  - Noise reduction
  - Hue preservation
- 8-bit YCbCr or raw 10-bit Bayer RGB output

IMAGE SENSOR SYSTEM BLOCK DIAGRAM

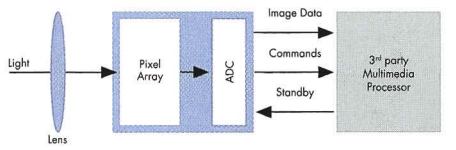
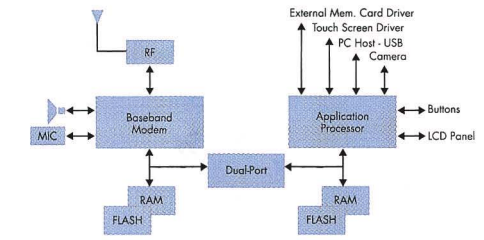


Image Sensors Selector Guide

Description	Pixel Size Squared	ADC	Optical Format
1.3 Megapixel	2.8µm	10-bit	¼"
1.3 Megapixel w/ Integrated SOC	2.8µm	10-bit	¼"
3 Megapixel	2.54µm	12-bit	⅓"

- No proprietary software dependencies while reusing subsystem IP across platforms
- Quick time-to-market for both platform and portfolio

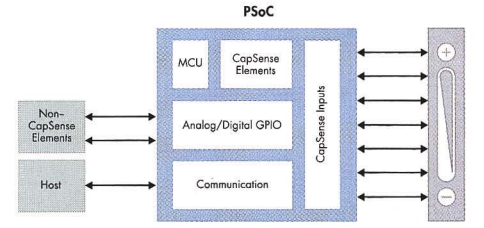
DUAL-PROCESSOR INTERCONNECT PHONE BLOCK DIAGRAM



Dual-Port Selector Guide

Density	Configuration	Maximum Speed	Package	I/O Voltage
256K	16Kx16	35 ns	6x6 mm fpBGA	1.8V to 3V
128K	8Kx16	35 ns	6x6 mm fpBGA	1.8V to 3V
128K	16Kx8	35 ns	6x6 mm fpBGA	1.8V to 3V
64K	4Kx16	35 ns	6x6 mm fpBGA	1.8V to 3V
64K	8Kx8	35 ns	6x6 mm fpBGA	1.8V to 3V

CAPSENSE CIRCUIT DIAGRAM



CapSense Device Selector Guide

Name	Flash	RAM	Additional Resources	Available Packages
PSoC™	8k	512	4 Digital Blocks, 2 Analog Blocks, Hardware I2C Master/Slave	16-SOIC 20-SSOP 28-SSOP 32-MLF
PSoC™	16k	1k	4 Digital Blocks, 2 Analog Blocks, Hardware I2C Master/Slave, Full-speed USB	56-MLF

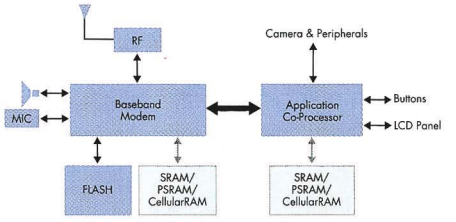
PSRAMs

- 100% compatible to SRAM
- Extra low-power features: Partial Array Refresh (PAR), temperature compensated self refresh Deep Power Down (DPD)

MoBL® SRAMs

- 35ns access time
- <1µA/Mb standby current

LOW-POWER MEMORY BLOCK DIAGRAM



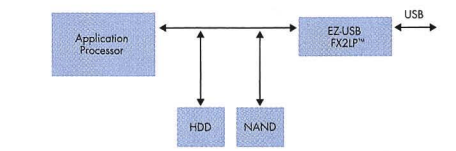
Low-Power Memory Selector Guide

Name	Interface	Vcc	Fastest Speed
CellularRAM™	Async SRAM, Sync, NOR Flash	1.8V	70 ns Async, 104 MHz Sync
PSRAM	Async SRAM	3V/1.8V	55 ns Async
MoBL® SRAM	Async SRAM	3V/1.8V	35 ns Async

#1 High-Speed USB Solution

- Lowest power USB 2.0 controller (bus/battery powered)
- Easy-to-use/flexible 2.0 architecture (48 MHz 8051core)
- Full driver support for mass storage/MTP
- Digital rights management support for WinCE

USB CONTROLLERS BLOCK DIAGRAM



USB Selector Guide

Name	Storage Interface	µC	Pin/RAM	Package
EZ-USB FX2LP™	ATA/ATAPI NAND Flash	8051 8-bit	16 Kbyte	56-pin QFN 48-pin BGA
EZ-USB AT2LP™	ATA/ATAPI	None	None	56-pin QFN
EZ-USB NX2LP™	NAND Flash	None	None	56-pin QFN
EZ-USB NX2LP-Flex	NAND Flash	8051 8-bit	15 Kbyte	56-pin QFN

support a different wireless standard (moving from GPRS to W-CDMA, for instance) or to upgrade the existing protocol (adding HSDPA to an existing W-CDMA baseband). Similarly, the application subsystems can be upgraded to support new capabilities independently of the wireless standard supported.

Connecting subsystems with a future-proof interface

To minimize the impact of each upgrade, the different subsystems must connect to each other through an interface that will be available on the next-generation chipset and will support future throughput needs.

Each subsystem is typically centered around a processing element (ASIC, DSP, GPP). Most of these processors today lack such an interface: serial standard interfaces are too slow to support new throughput needs such as 3G, Video or 802.11; high-speed interfaces involve proprietary protocols that are incompatible across chip vendors and involve long software changes and validation for every update.

The memory bus provides a good candidate for an interconnect – all processors will always support a memory interface and the bandwidth achieved is well above current requirements (290 Mbps for a 55 ns access time on an x16 bus). Two memory buses can be connected together using a dual-port interconnect.

A dual-port interconnect is a memory-mapped IC that allows two processing elements to access a shared memory space independently. It allows processing elements to exchange data through their memory bus, simply using standard write and read operations.

A dual-port is the most flexible interprocessor interconnect available. By offering a standard SRAM interface that connects with the existing memory bus, it allows an existing processor to interface with almost any other processing element with high bandwidth. It also simplifies and reduces communication software overhead.

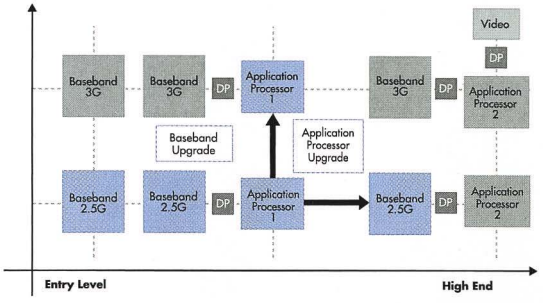
The dual-port enables a system upgrade by adding a processing element to the existing architecture. For example, adding a new processor causes limited changes since the existing processor only perceives additional memory on its bus. One port of the dual-port is connected to the existing processor's memory bus and the other port is connected to any device with an SRAM interface, including any processor or modem.

MoBL® Dual-Ports enable modular design strategy

Cypress's low-cost MoBL® (More Battery Life®) Dual-Ports are designed specifically for mobile platforms, combining high-performance dual-port architecture with industry-leading, low-power technology to conserve battery life.

More than just enabling upgrades with short development time, modular architectures maximize the reuse of IP developed for specific subsystems. A whole portfolio can be built out of the different blocks available, with the use of similar subsystems across multiple platforms.

The figure below describes a handset portfolio based on this modular approach. A single baseband chip is used in the simplest designs. It is then enhanced multiple times to create several new products by the addition of different application processors via a dual-port interconnect. The dual-port interconnect enables two completely different applications processors to be added to the



Example of a handset portfolio using a modular architecture strategy

baseband processor with minimal changes, allowing market and cost differentiation of the new platforms.

When the next-generation baseband is developed, the previously developed application IP can be reused by simply upgrading the communication subsystem. The existing architecture can even be exported easily from one band (GPRS for instance) to another (CDMA) with minimum changes to software and system architecture. ■

CYPRESS HANDSET SOLUTIONS: WHOLE PRODUCT SUPPORT

Application Notes/White Papers

- 3 Megapixel Flash Implementation
- Implementing Interprocessor Communication Using MoBL® Dual-Port
- Interfacing MoBL Dual-Port to TI OMAP1710 Application Processor
- Interfacing MoBL Dual-Port to Intel® PXA270 Application Processor
- Cypress USB 2.0 Mass Storage Device Driver for Windows
- Capacitive Key Scan
- Capacitive Front Panel Display

Technical Articles

- Using Memory Buses To Build Modular Portable Architectures
- Capacitive Sensing in Cell Phones
- Developing Low-cost Modular Handset Architectures Using Dual-Port Interconnects

Reference Designs

- High-speed USB 2.0-to ATA/ATAPI
- CY4618 EZ-USB NX2LP™ Reference Design Kit
- CY4619 EZ-USB FX2LP™ MTP Solution

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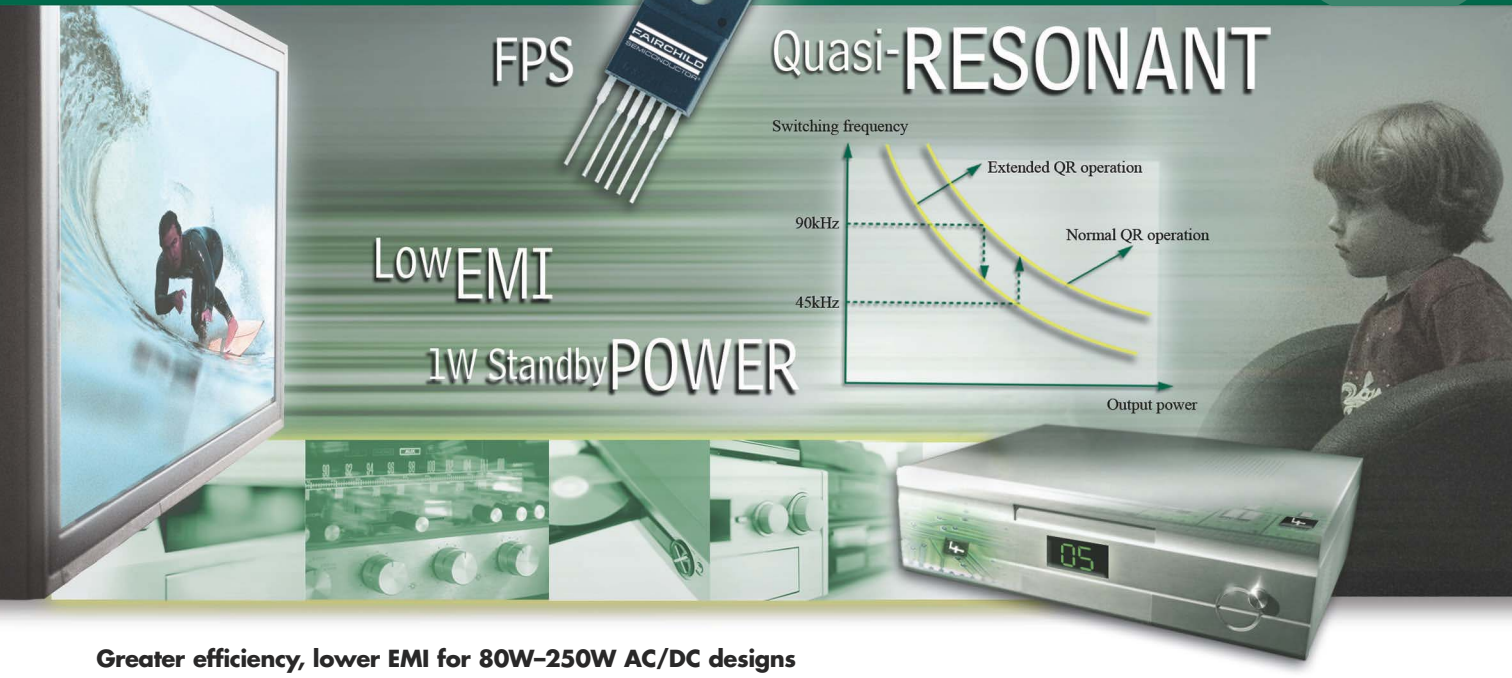

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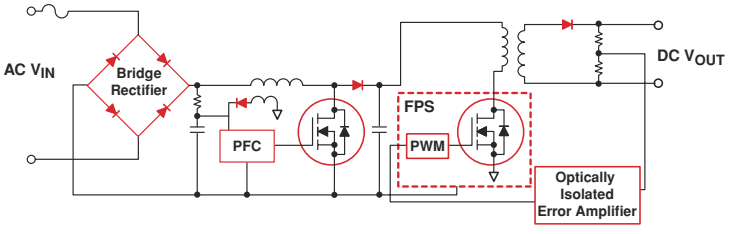
For power supply designs in noise-sensitive applications, choose Green Fairchild Power Switch (FPS™):

- Optimized for quasi-resonant converters (QRC)
- Integrated PWM and avalanche-rugged SenseFET™
- Advanced burst-mode operation for under 1W standby power consumption

You'll see greater efficiency, with fewer parts, using Fairchild's QRC SMPS solutions.

Part Number	$P_{O(MAX)}$ (W) 85-265V_{AC}	Peak Current Limit (A)	$R_{DS(ON)}$ Max (Ω)
FSCQ0565RT	60	3.5	2.2
FSCQ0765RT	85	5	1.6
FSCQ0965RT	110	6	1.2
FSCQ1265RT	140	7	0.9
FSCQ1465RT	160	8	0.8
FSCQ1565RT	170	8	0.7
FSCQ1565RP	210	11.5	0.7

Green FPS for quasi-resonant switching converter



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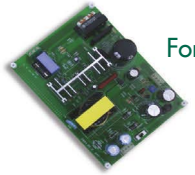

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the power franchise™

BY DANIS CARTER • TYCO HEALTHCARE

Skunkworks project ends up smelling like a rose

A fellow project team member encountered difficulty stabilizing a pneumatic valve developed from a skunkworks effort. His voice-coil-driven valve offered a new technology to our industry, and we were looking at the feasibility of using it as an exhalation valve in a new medical ventilator. The voice-coil motor would permit a fast lung-ventilator response to patient-initiated breaths, easing the patient's work of breathing. The fast prototype valve had the undesirable effect of overshooting the targeted patient pressures. The new valve not only had technical difficulties, but also plenty of detractors from management who wanted to use a slower, more proven valve. I have always pulled for the Sisyphus engineer, and I wanted to help him push his valve to the top of the mountain.

The mechanical-engineering group resisted my recommendations of attaching a transducer to the armature and feeding back the oscillations to the motor driver, correcting for the overshoot. They felt that it was too involved to attach a sensor and that a sensor might add too much weight to the motor's armature. The valve's poppet attached directly to the armature, and significant weight would affect performance. After designing the valve's power amplifier, I thought that a feedback signal would be a natural solution. The valve engineer attempted to stabilize the assembly with springs and pneumatic dampening devices, but the dampening devices deleteriously affected the valve's linear performance.

While discussing a circuit with a lab technician, I noticed a collection of small bar magnets holding papers to his bench lamp. I had for years seen these magnets but suddenly realized that they could effect a solution for the valve. When everyone had gone home for the day, I made a "midnight requisition" of a bar magnet and super-glued it to the bottom of the valve's armature. I then wound a bunch of magnet wire around a tiny pot-core bobbin and positioned it so that the magnet could travel through the bobbin's center. I now had a homemade velocity sensor. After performing some open-loop tests for velocity sensitivity, I closed the loop with a velocity amp, feeding the signal back to the power amp's negative input. I connected tubing, an air source, and a pressure sensor to the valve.

Using an oscilloscope to monitor the pressure sensor, I observed the airway-pressure changes when I applied a step function to the valve driver electronics. The velocity feedback immediately improved valve stability, but the system still needed some refinement. I placed a variable resistor in the velocity amplifier's feedback loop to allow control of the dampening, which I subsequently demonstrated to the valve designers by tuning in overdamped, critically damped, and underdamped responses. The stark performance improvement with the crude bar magnet and hand-wound coil convinced management that the approach was practical and that the voice-coil-driven valve was feasible.

Eventually, we refined the system to allow software-gain control of the feedback signal and usage of standard magnetic parts for the velocity signal. We found that controllable gain was desirable for the dampening because different airway-pressure levels required different dampening levels. After answering a bunch of "how-can-you-do-that?" questions from management, the valve quickly rose from a skunkworks project to full-development status.

This case was another one in my career in which I pursued an unpopular approach that all players endorsed once it proved successful. It's interesting how a few disparate parts, such as a paper magnet, pot-core bobbin, magnet wire, and super glue, can form a breakthrough. I eventually received a patent for this system, and the valve and electronics are in 23,000 ventilators across the globe. EDN

Danis Carter is a principal engineer at Tyco Healthcare. He also serves on EDN's *Editorial Advisory Board.*

DANIEL VASCONCELLOS

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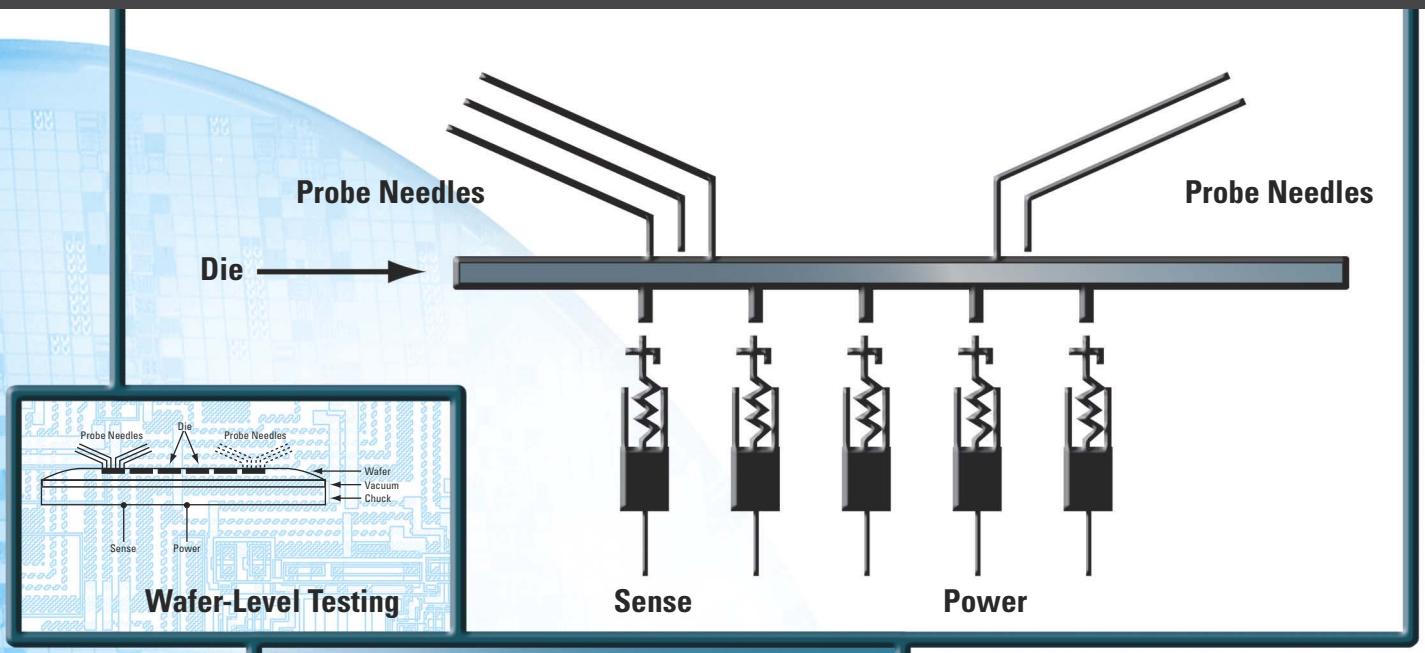

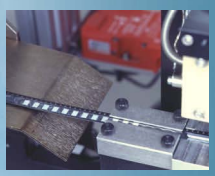

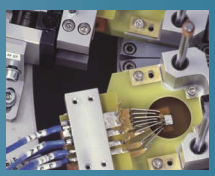

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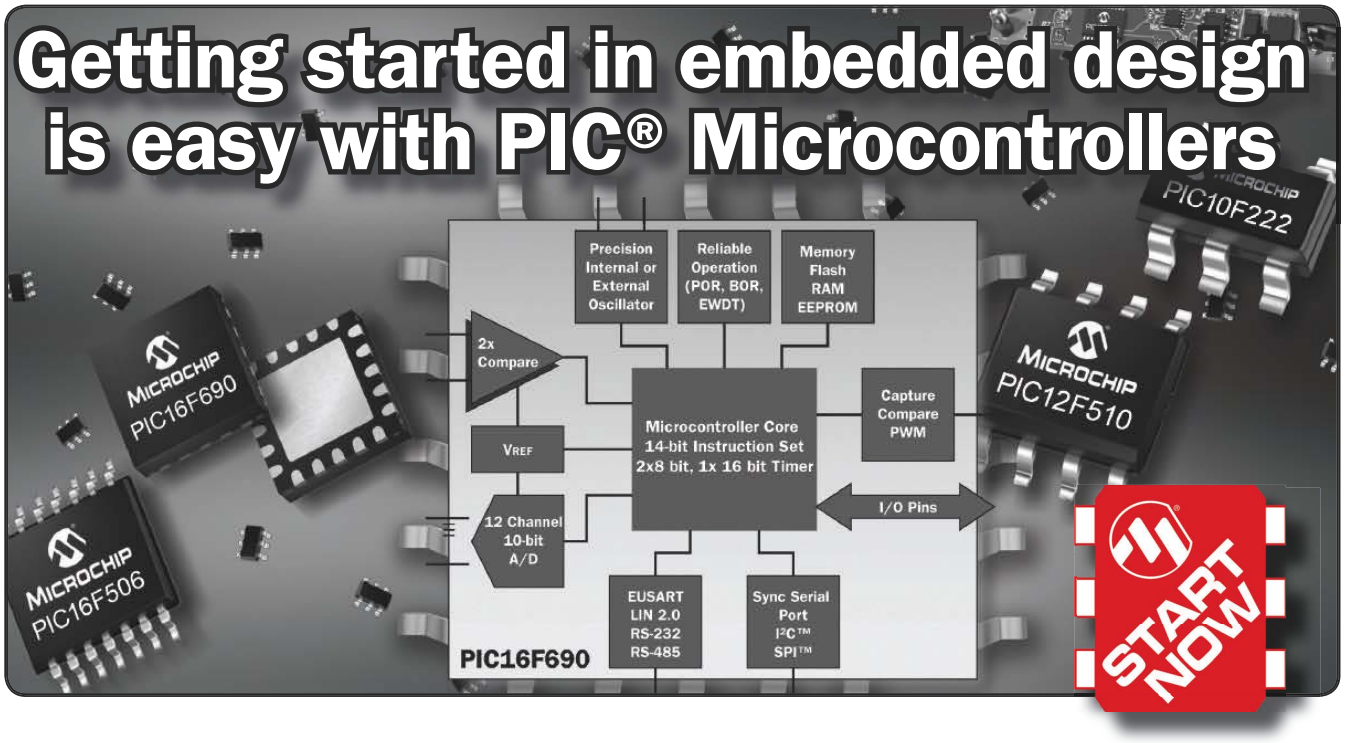

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BY ROBERT CRAVOTTA • TECHNICAL EDITOR

OPERATING ALONE

AUTONOMOUS SYSTEMS ARE SHOWING UP IN MORE PLACES. COMPETITIONS SUCH AS THE DARPA GRAND CHALLENGE ARE INCREASING THEIR VISIBILITY.

Figure 1 Stanford Racing Team's autonomous vehicle, "Stanley"—a reinforced Volkswagen Touareg with a custom drive-by-wire system, a sensor rack, and a computing system—won the 2005 DARPA Grand Challenge (courtesy Stanford Racing Team).

The DARPA (Defense Advanced Research Projects Agency) Grand Challenge is a highly publicized competition to encourage the development of fully autonomous vehicles that can complete an off-road desert course. On Oct 9, 2005, the Stanford Racing Team, from a field of 23 competitors, claimed the $2 million prize for its vehicle, which completed a 132-mile desert course in California with no human assistance once it left the starting gate (**Figure 1**). Four other fully autonomous vehicles completed the course with a slower time.

The vehicles had to follow a prescribed course route, provided as a GPS (global-positioning-system) way-point file; avoid obstacles; and negotiate turns in desert conditions while traveling at speeds relevant to a military context (see **sidebar** "Racing in the desert"). The actual course was secret until just before the competition, so that each vehicle would be running the course for the first time. The competition aims to yield the precursor of deployable and fully autonomous supply convoys that can travel through hostile territory and eliminate the risk to drivers of such vehicles in areas of conflict.

Autonomous systems allow human operators to perform tasks in environments that are hazardous to humans, including outer-space and underwater environments, without requiring continuous human guidance. In these types of environments, a high degree of autonomy is desirable, especially when it is impossible to avoid communication delays and interruptions. Although competitions such as the DARPA Grand Challenge help publicize and push the technological enve-

AT A GLANCE

- Autonomous systems can operate in uncertain environments without continuous human intervention.
- Autonomous systems combine sensors, actuators, and detection and decision logic in a closed-loop control configuration.
- The more uncertain the operational environment is, the more important system integration and field testing become.
- Development tools targeting autonomous systems provide emerging opportunities for tool providers.

lope for fully autonomous vehicles, such machines represent only a relatively small and extreme edge of the possible spectrum of these systems (see **sidebar** "Other competitions").

The current state of electronics-based autonomous systems requires some direction from a human operator. The extent to which the system can operate in uncertain environmental conditions without human intervention determines the level of autonomy the system supports. There is an increasing number of embedded systems with varying levels of autonomy that are invisible to human operators.

Examples of invisible, semiautonomous systems include antilock-braking systems available in many contemporary cars. Machines for washing and drying clothing can exhibit autonomous behavior by being able to automatically adjust the machine's operation based on sensing the condition of the clothing during operation. Remote-controlled aircraft and underwater robots are partially autonomous, because there is no way to transmit relevant operational and control data between the operator and the vehicle to adjust for sudden or rapid shifts in the environment.

AUTONOMY

For an autonomous system to be able to successfully operate in an unpredictable environment, it must be able to sense and receive information about its operating environment. Another essential capability for autonomous systems is to be able to interact with the environment through a set of actuators. Detection, decision, and control processing, often in the form of software, bridge the sensor and actuators to form the brains of the autonomous system. The whole system operates in a closed-loop fashion, so that the system can detect and adjust for the effect its own actions have upon the environment. An open-loop system, or one that is missing one of these capabilities, is not an autonomous system.

The amount of environmental uncertainty autonomous systems can handle ranges from a small, well-defined set of changes, such as in a factory setting with strict tolerances and control on the environment, to a large set of widely uncertain conditions, such as in the case of autonomous vehicles that are traversing desert terrain for the first time.

Likewise, the level of autonomy a system can manifest can vary widely (**Figure 2**). For example, once you activate a factory system, it can operate virtually indefinitely without human intervention. At the other extreme, a semiautonomous system, such as an underwater robot, may receive continuous human intervention with regard to course position and task control, but it may receive no human intervention for fine-positioning control. Also, by making the fine control autonomous, the operator can function at a higher abstraction level and focus more on the mission objectives.

The types of commercially available visionlike sensors include passive and active sensors (**Reference 1**). All sensors have strengths and weaknesses, and it is important that designers choose the right sets of sensors to cover the aspects of the environment that the system will encounter. Passive sensors, such as single-vision, stereovision, and thermal cameras, detect information by sensing what is in the environment, such as light and thermal radiation. Passive sensors are susceptible to too little or too much ambient energy in the environment. Active sensors, such as radar sensors, LIDAR (light-detection-and-ranging) sensors, and infrared and ultrasonic transducers, detect information by transmitting energy into the environment and sensing the amount of and the timing of the reflection of that energy back to the sensor.

In addition to using visionlike sensors, mobile autonomous systems may rely on additional sensors, such as GPS and IMU (inertial-measurement-unit) sensors, to detect the system's position and attitude in the environment. Mobile systems that can work in a constrained environment, such as iRobot's Roomba, employ external transmitters, such as infrared, so that the mobile system can sense and interpret them as a physical boundary.

The sensor-processing, feature-detection, and decision software represent the largest area for innovation in autonomous systems. The software must be able to reduce and abstract key features from the sensor data and be able to correlate the data if there are multiple types of sensors working in concert. Knowing what features to detect in the sensor data is application-specific. In the case of the desert race, the vehicles needed to be able to identify and navigate around stationary obstacles. However, they needed

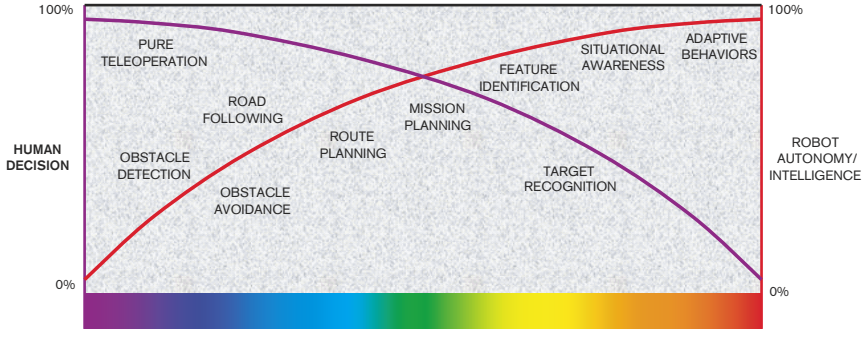

Figure 2 The amount of human decision and intervention an autonomous system will need varies. As detection, planning, and decision software improves, these systems will be able to move more to the right of the spectrum of autonomy (courtesy JAUS).

neither to identify nor to predict the movement of those obstacles.

An important ability for autonomous systems is detecting and correcting for anomalous or boundary conditions. The response to each type of condition is also application-specific. Sometimes, the correction is internal to the system, such as repositioning, or it reinitializes the system; other times, the correction is external, such as raising an alarm for a human to intervene. An emerging area for com-

RACING IN THE DESERT

The entries in the DARPA (Defense Advanced Research Projects Agency) Grand Challenge employed a range of off-the-shelf sensors, including LIDAR (light-detection-and-ranging) sensors, radars, single-vision and stereovision cameras, color and thermal cameras, ultrasonic transducers, GPSs (global positioning systems), and IMUs (inertial-measurement units). Most entries employed multiple, complementary sensor systems to provide enough coverage for the vehicle to sense the environment, obstacles to avoid, and attitude and positioning.

Only a few teams developed custom sensing equipment. Most notable among the custom sensors was a LADAR (laser-radar) system that Team DAD (Digital Auto Drive) developed and successfully demonstrated during the competition (Figure A). The unit generates its own light and uses a proprietary filter to reject sunlight, so it works well under all lighting conditions. The unit can see through fog and heavy rain by ignoring early reflections.

The LADAR system employs 10 DSPs that process data from 64 lasers for terrain mapping and object detection, which solves some problems the team experienced when using a camera system in the first Grand Challenge event. The 64 lasers all rotate at 600 rpm in a drum mounted atop the vehicle driver cab. Because the whole system spins, dust and rain spin off the unit as it rotates. Team DAD did not have enough time before the competition event to develop the LADAR data processing to perform localization during loss of the GPS signal.

The PVHS (Palos Verdes High School) Road Warrior team also developed a custom sensor. The ground mouse, which the team did not get to successfully demonstrate at the race, uses a narrow, spectral, filtered light source; a detector array; and a modified Newtonian optic system to make ground measurements every 2 msec. The ground mouse works with the IMU. This setup allows the control system to work with an accurate estimate of the vehicle's position when the GPS signal drops.

The experience at the competition demonstrates that commercially available sensor technology is sufficient for fully autonomous systems and is not the source of the major challenges for developing these types of systems. Actuators for throttle and steering control were generally straightforward and did not represent the most challenging areas for these fully autonomous vehicles. Most difficult, not surprisingly, is implementing the software detection, decision, and control algorithms. Each team entry emphasizes its software and vehicle intelligence, supporting the assertion that the event is largely a software competition. The teams develop their software using C/C++ code, hand-coded assembly, or Java. Details about each team's sensors, actuators, and control, planning, and decision software are available as technical papers at www.darpa.mil/grandchallenge.

Lessons participants learned from the event include the importance of the task and system-level integration effort. Teams that did well in the event logged hundreds of hours and miles of field operation. The integration effort is essential to making the system reliable under the various environmental conditions these vehicles had to endure over the 132-mile course. Team DAD's vehicle stopped short of the finish line in part because the team did not have enough time to harden the vehicle for desert conditions. In its case, the removable mounting on top of the driver cab loosened and contributed to a set of cascading errors that led to the team's pulling the entry before it crossed the finish line.

The short time frame to prepare for the competition amplified the need for teams to use off-the-shelf parts wherever possible. Spending more time developing custom hardware systems meant spending less time in integration and field-testing. This trade-off is evident in the teams' processor choices. Most vehicle-sensor and -control systems used general-purpose processors from Intel, AMD, Freescale, and Apple. A few teams used Texas Instruments DSPs, Microchip PIC controllers, or National Instruments controllers. It is unlikely that a production version of these autonomous vehicles would use general-purpose processors, because they are less efficient and more costly than DSPs and microcontrollers for such tasks. But for prototyping, general-purpose processors allowed the teams to more quickly get to field-testing and do that testing for a longer time before the event.

Figure A The custom LADAR system sits atop the vehicle driver cab and spins at 600 rpm to provide accurate terrain data (courtesy Team DAD).

plex autonomous systems is the ability to learn; it would include adjusting decision strategies based on the environment, especially for unanticipated boundary conditions.

Although full autonomy is a goal, employing such systems in complex environments is a long way off. The practical response to this situation is incremental autonomy, in which designers continually expand and improve the abilities of a system over multiple iterations. This approach may manifest itself as a system that begins with an operator's making all of the decisions through remote control and, with each iteration, making fewer actions or decisions. Before the system takes over a decision, an earlier iteration may include the system's notifying the operator of, rather than acting on, the condition.

INITIATIVES AND TOOLS

The JAUS (Joint Architecture for Unmanned Systems) is an initiative for developing a message-based architecture for upper level interfaces of unmanned systems, so that independent teams may eventually and more easily interoperate with each other. The goals of the initiative are to reduce the development and integration time, as well as the life-cycle costs, of autonomous systems. The initiative specifies a framework for technology insertion and how to accommodate the expansion of systems with new capabilities. It also specifies performance-based requirements about what to build but avoids defining how to build it.

JAUS identifies that manufacturers currently build the subsystems that are common to all unmanned systems from scratch for each system. They cannot easily incorporate the performance gains they make in one system into different systems with similar requirements. The initiative champions a component-based, message-passing architecture that specifies data formats and methods of communication among computing nodes. It defines messages and component behaviors that are independent of technology, computer hardware, operator use, and vehicle platforms and isolated from the mission.

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The Unmanned Aerial Robotics Initiative involves people from various laboratories that meet regularly to exchange experience and knowledge, believing that experience they gain in one project is often useful to other projects. The initiative maintains a Web portal at aero.epfl.ch and supports students developing projects in this field.

Software-development tools for autonomous systems lag behind the sensor and actuator options. However, the aerospace and the military markets are driving the tools to handle the complexity that autonomous systems exhibit. In addition to homegrown tools, commercial-modeling tools, such as those from The Mathworks, are supporting multiple-domain modeling with tighter integration between the sensor and the control aspects of the system model. Tools, such as those from National Instruments, are improving to support prototyping to embedded targets, which simplifies integration and communication between distributed intelligent nodes. Real-Time Innovations' tools target systems with real-time distributed data requirements.

Simulation, including hardware-in-the-loop simulation, is an opportunity for simulation-tool providers (**Reference 2**). The sensor fusion, or the correlation of data from multiple and possibly different sensors, which complex autonomous systems require, presents significant processing requirements on simulators—especially systems with real-time, closed-loop requirements.

Strong project management is essential when developing autonomous systems because of the wide range of engineering disciplines that must work together to design these systems. As an example, the Stanford Racing Team comprised four major groups. The vehicle group oversaw the modification and developments, including the drive-by-wire systems, as well as the sensor and computer mounting, as it related to the core vehicle. The software group handled all the software, including the navigation software and the health-monitoring and safety systems. The testing group was independent from the other groups and was responsible for testing the components and the system as a whole. The communication group managed media relations and fundraising activities.

The complexity of data sharing and maintaining coherency becomes complicated with development teams that are geographically distributed. The PVHS (Palos Verdes High School) Warrior Team not only had to deal with language, time-zone, and shipping delays when working with a group in the Ukraine for the motion-control system of its entry, it

OTHER COMPETITIONS

There is a lot of room for improvement in autonomous robots. One way to spur innovation and speed development for these systems is through competitions such as the DARPA (Defense Advanced Research Projects Agency) Grand Challenge. The aviation industry received a boost by a similar competition that offered $25,000 for the first flight between New York and Paris. This challenge was the motivation that spurred Charles Lindbergh on his historic flight.

There is a wide variety of robot contests available to compete in or watch. The FAQ at www.robots.net/rcfaq.html lists information on robot contests and competitions, many of which include cash prizes. The site lists a schedule of 87 contests from October 2005 through September 2006. Some of these competitions, such as the AUVSI (Association for Unmanned Vehicle Systems International) Aerial Robotics Competition, include prizes that increase each year until a team wins the competition.

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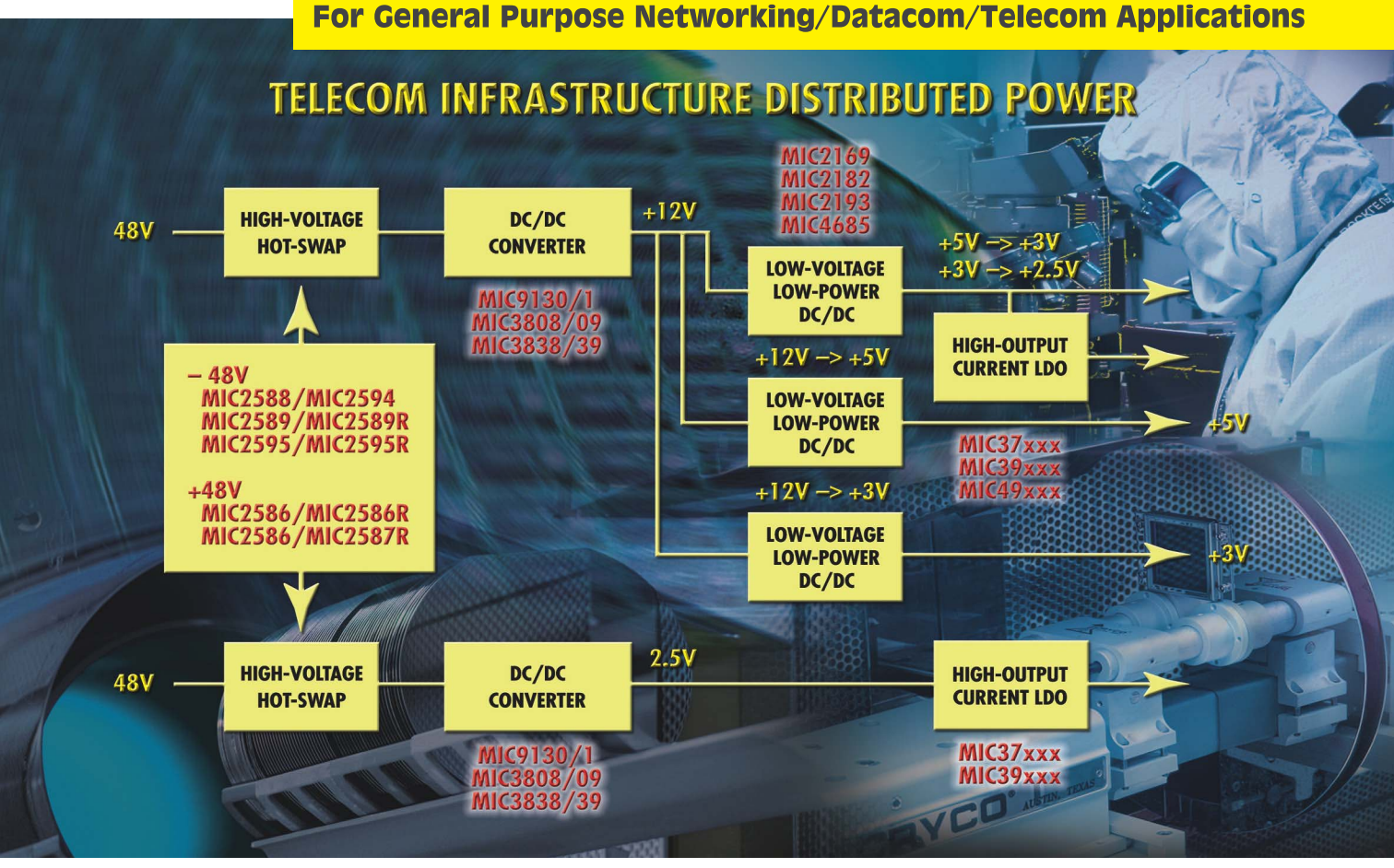

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also had to be aware of import/export regulations for the data it was sharing.

For some autonomous-system designs, a straight if-then decision tree is sufficient, but, as these systems continue to grow in complexity, there may be an opportunity for decision-rule-management tools. Database management may become more important as these systems evolve from just detecting features in the environment to recognizing features, so that they can better predict and anticipate changes in their environment.

There is a growing opportunity for autonomous systems that can interact with the physical world and manipulate physical objects. Today, autonomous systems take direction, directly and indirectly, from a human operator. Some of these systems are obvious to the end user, but many of them, such as the growing number of automobile-safety features, augment and abstract some aspect of controlling a system so that the operator can focus on higher level tasks and functions. Also, given the success of connected devices and computing networks, it is not a stretch to expect future independent and autonomous systems to work not just with human operators but also cooperatively with each other. **EDN**

FOR MORE INFORMATION

AMD
www.amd.com

Apple
www.apple.com

AUVSI (Association for Unmanned Vehicle Systems International)
www.auvsi.org

DARPA Grand Challenge
www.darpa.mil/grandchallenge

Freescale
www.freescale.com

Infineon
www.infineon.com

Intel
www.intel.com

iRobot
www.irobot.com

JAUS (Joint Architecture for Unmanned Systems)
www.jauswg.org

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www.ni.com

Real-Time Innovations
www.rti.com

Stanford Racing Team
www.stanfordracing.org

Team Cornell
www.darpa.mil/grandchallenge

Team PVHS Road Warriors
www.darpa.mil/grandchallenge

Texas Instruments
www.ti.com

Velodyne Acoustics (Team DAD)
www.velodyne.com

Xilinx
www.xilinx.com

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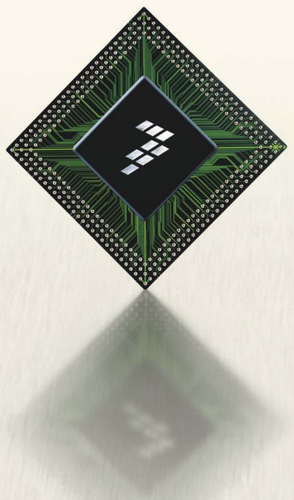

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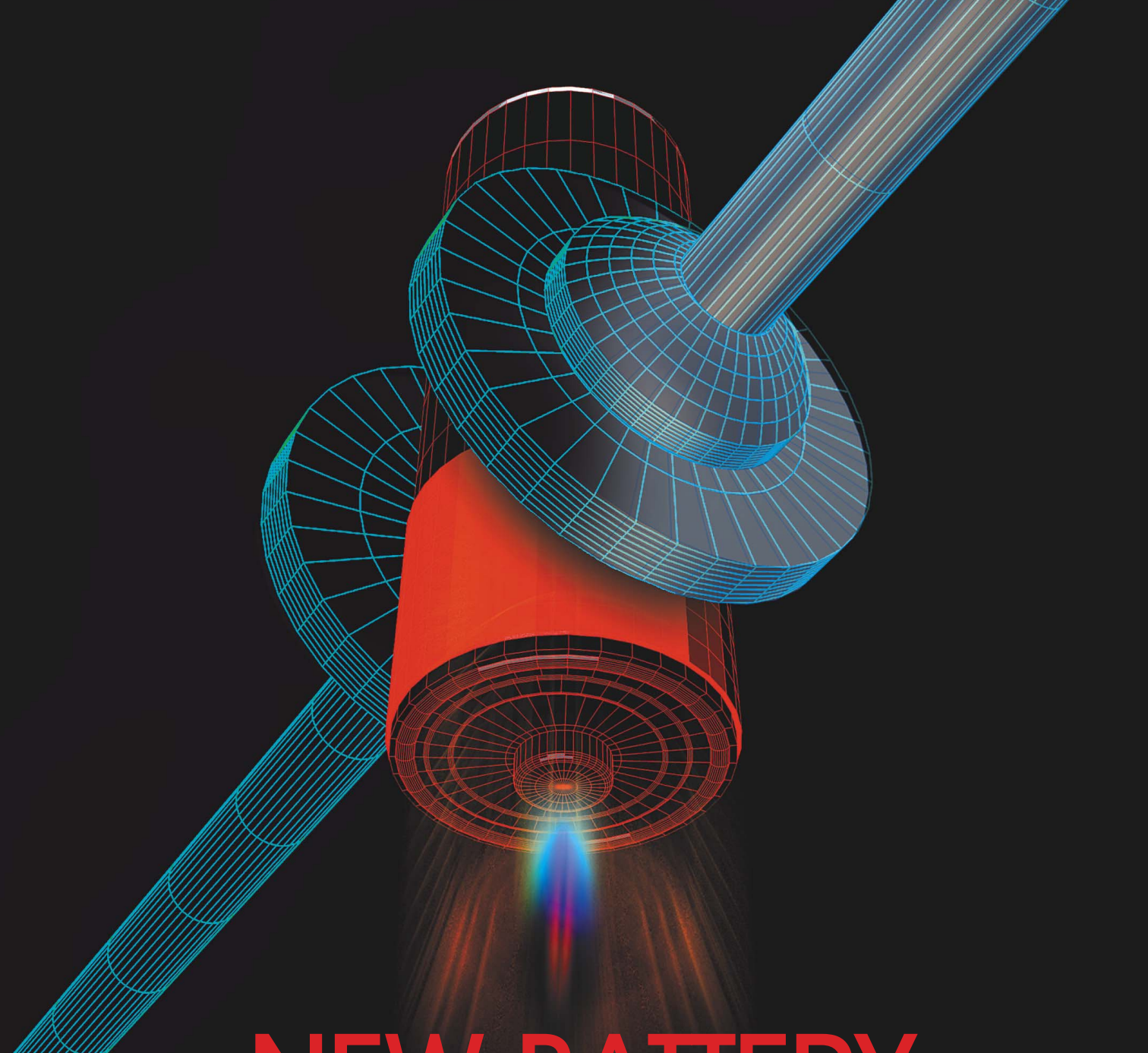


NEW BATTERY TECHNOLOGIES HOLD PROMISE,

PERIL FOR PORTABLE-SYSTEM DESIGNERS

MARGERY CONNER
TECHNICAL EDITOR

FOR THE NEAR FUTURE, MOST PORTABLE SYSTEMS WILL HAVE TO RELY ON SOME FORM OF THE NOW-VENERABLE LITHIUM-ION BATTERY. FORTUNATELY, LITHIUM-ION CELLS ARE IMPROVING IN COST, ROBUSTNESS, AND EVEN ENERGY CAPACITY. BUT BEWARE THE PERILS THAT "CLONE" BATTERY PACKS CAN POSE FOR YOUR SYSTEM.

For portable systems relying on a battery or a battery pack, the ever-increasing complexity and speed of the system's ICs and the resulting increase in power requirements are problematic: Although ICs can surf the processing and speed wave of Moore's Law, battery technology has improved at a much slower pace. The increase in energy capacity for a lithium-ion cell has little more than doubled in 10 years, from 280 Whr/l (watthours per liter) in 1995 to 580 Whr/l in 2005. Compare this figure with the IC's ability to double its complexity every 18 months, and you can see the mismatch between power need and power capacity for portable devices.

Although batteries don't enjoy the gee-whiz aura of the IC, lithium-ion technology has nevertheless made significant advances. By changing the chemical formulation of the cathode and anode, lithium-ion-battery manufacturers are tweaking cells' energy capacity, as well as cell cost and robustness. However, even as vendors make advances, variations will emerge. System designers will need to pay attention to battery formulations and be aware that battery charging and output voltages are changing, affecting system requirements.

Lithium ion is not the only type of rechargeable cell that battery packs use. Older but still popular types are NiMH (nickel metal hydride) and NiCd (nickel cadmium). Lithium ion, which manufacturers introduced in 1991, is the newest technology, but it has taken over the field with its combination of relatively low cost and high energy density (**Table 1**). (For a definition of battery terms, such as "cell" and "pack," see **sidebar** "A battery of definitions.")

What's been driving the change in lithium-ion chemistry? In addition to the need for higher power density, battery manufacturers want a cheaper formulation as well as a safer, more robust mix. Tweaking the lithium and other chemicals in a battery cathode affects the battery cost, capacity, ruggedness, and voltage.

In today's lithium-ion cells, which typically come in a 18650-size cyclindrical package, the anode is a graphite mixture, and the cathode is a combination of lithium, nickel, and cobalt. When lithium batteries first became available in the 1990s, cobalt was relatively inexpensive, and its price was stable. But cobalt prices began to rise at the end of the decade, and battery manufacturers

AT A GLANCE

- Plan on lithium-ion cells' continuing as the dominant power sources for portable consumer electronics, such as laptops and cell phones.
- Some lithium-ion batteries will change both their charge voltage and their output voltage.
- Higher voltages, which can damage both older battery packs and device electronics, will necessitate battery authentication to protect users from substituting old and potentially unsafe battery technologies.

worked on new cathode materials that moved away from cobalt.

According to Robin Tichy, product-marketing engineer with Micro Power, a battery-pack developer that incorporates cells from several manufacturers in its packs, "The road map for lithium-ion batteries based on current $LiCoO_2$ (lithium-cobalt-dioxide) formulations is that vendors are phasing out 2 Ahr, 2.2 Ahr is currently in production, and 2.4 Ahr is coming into production." Tichy says that manufacturers are evaluating 2.6-Ahr technology and planning 2.8-Ahr technology. "When you hit 3 Ahr, you reach the theoretical maximum for lithium cobalt dioxide in the 18650 cell," she says.

In addition to its relatively high cost, Tichy points out, cobalt is chemically more volatile than other potential cathode materials, such as nickel and manganese. "Nickel is less volatile, both economically and chemically, than cobalt," she says. "However, it's also much less efficient at charge cycling. Manganese is cheap and safe with good [high-current]-rate capabilities. Manganese's drawback is that it has poor energy density and is slightly soluble in an electrolyte."

The first alternative to lithium cobalt dioxide that will appear in an 18650 cell will have a cathode with a solid solution of NCM (nickel-cobalt manganese). Manganese and nickel replace some, but not all, of the cobalt in a partial phasing-out of the cobalt material, resulting in a better battery price but no additional energy capacity.

Because the cell voltage is due to the difference in the electrical potential between the anode and the cathode, a change in cathode material changes the cell-output voltage. Although the NCM formulation increases cell voltage by only about 0.1V, that increase is still enough to make an impact on the host design. And NCA (lithium-nickel-cobalt-aluminum dioxide), a formulation coming hot on the heels of NCM, will have an even greater differential.

Due at the end of 2006, NCA is another formulation from Panasonic. The formulation is similar to NCM, but it has more nickel, and aluminum replaces manganese, which also connotes less volatility and explosive potential, says Tichy. "The other advantage is that the more nickel you put in, the higher the capacity will be." At 620 Whr/l, NCA provides the industry's highest energy density. Correspondingly, the cell's output voltage will probably be 3.6V.

In addition to the higher output voltages of the new battery chemistries, the batteries charge at a higher voltage, posing a problem for systems that provide a system charger that must be able to distinguish the battery type before charging at the higher voltage. Brian Barnett, managing director at Tiax LLC and conference chairman of the Portable Power 2005 conference, says, "Rather than having a simple world when there were not a lot of versions of lithium-ion batteries, we're headed in the direction of having numerous versions that don't have the same terminal characteristics. If you took today's 4.2V lithium-cobalt-dioxide technology and you accidentally put that into a charger that was not smart enough to recognize the different chemistry, you could have a very serious incident." System designers can guard against a user's charging cells with the wrong voltages by implementing authentication circuitry in their pack (**Reference 1**).

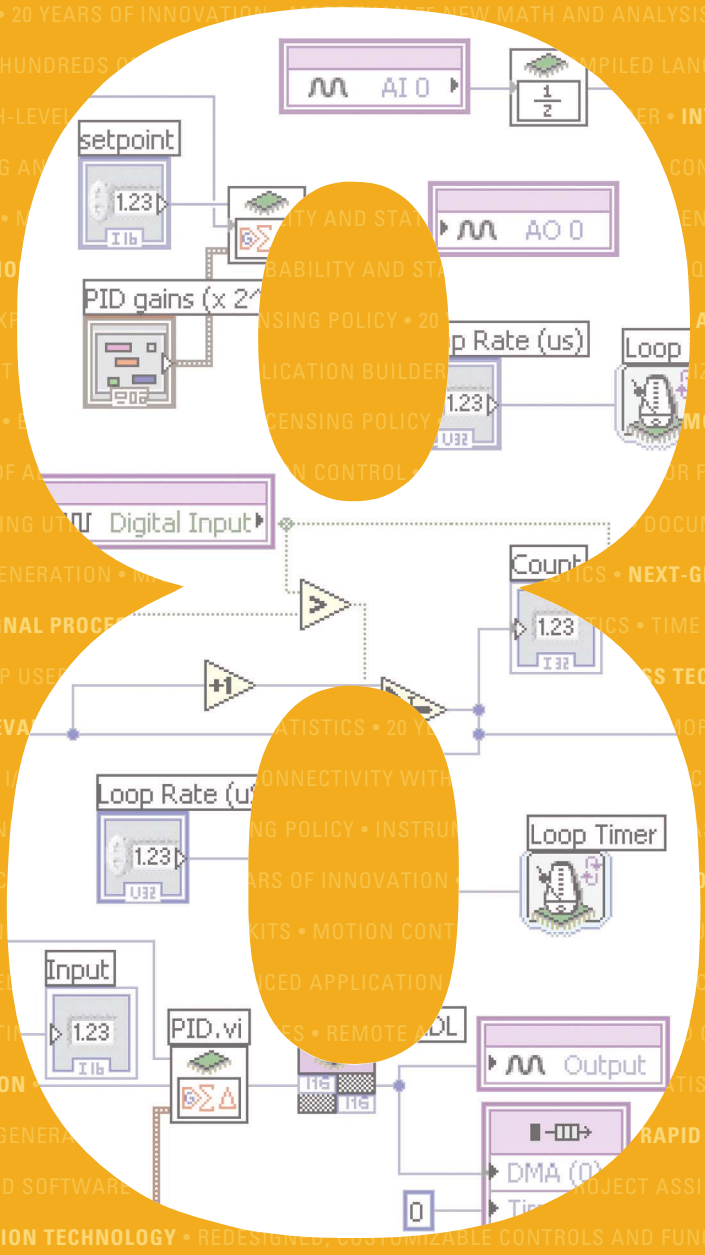
Dave Heacock, vice president of Texas Instruments' portable-power-management business, sees a lot of electronic-system designers trying to squeeze every last bit of power from the system battery pack. "The battery can be a point of differentiation in the marketplace if it's done well, and the extra little money you pay there goes a long way toward making your system sell," he says. The new lithium-ion-battery formulations are attractive but also can introduce variations into battery-performance characteristics that weren't there before. "A lot of the battery manufacturers' efforts are in trying to squeeze more out of the same space and in trying to make the cell safer. When they first develop a cathode or an anode, they often have some difficulties in having it perform to the same level as some of the more mature chemistries," he says. The

BATTERY MANUFACTURERS' EFFORTS ARE IN TRYING TO SQUEEZE MORE OUT OF THE SAME SPACE AND IN TRYING TO MAKE THE CELL SAFER.

TABLE 1 MOST POPULAR RECHARGEABLE-BATTERY TECHNOLOGIES AND THEIR CHARACTERISTICS

Battery chemistry	Energy density (Whr/kg)	Charge cycles	Self-discharge rate (%/month)	Special disposal
Nickel metal hydride	60 to 120	200 to 1000	30	No
Nickel cadmium	45 to 80	700 to 1300	20	Yes
Lithium ion	110 to 250	500 to 1000	0 to 10	Yes

Courtesy NanoMarkets, "Micro Power Sources: Opportunities from Fuel Cells and Batteries for Mobile Applications," September 2005.



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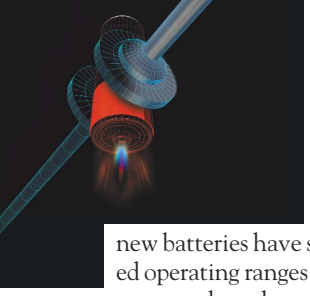

new batteries have such severely restricted operating ranges that system designers may need to choose a battery pack that has built-in battery-management circuitry, such as authentication.

But system designers can't just hand off all battery-pack decisions to their battery-pack vendor. Heacock cautions, "Make sure you know what's inside," especially regarding the cells themselves. The process technology for lithium-ion cells, especially among the long-time companies, such as Sanyo, Panasonic, and Sony, are well-established, and production results are repeatable. However, for newer battery manufacturers, often the hungry Chinese manufacturers, variance in battery specifications, such as temperature versus discharge rate, can vary wildly from cell to cell. "Newer companies compete on price, so make sure you know what you're getting for that price. Ask how stable their cell-to-cell variance is," says Heacock.

A BATTERY OF DEFINITIONS

***Lithium ion*: This technology is the most popular rechargeable-battery technology for most consumer products. Lithium is the lightest metal and provides the highest energy density of all battery formulations; however, it is also highly reactive and unstable during charging. Batteries almost universally use lithium ion, a more stable form. However, its ionic form is still explosive in certain conditions. (For a graphic depiction of lithium-ion cells subjected to overcurrent conditions, see the "Techflicks" sidebar in Reference A.)**

Lithium-polymer cells have similar specifications to those of lithium-ion, but they feature a semirigid and thin form factor with only half the lifetime. Their "flexibility" is often misleading, because lithium-polymer cells should remain flat when you install them in a device, not even bending for installation in the battery system. They are also more expensive (Reference B).

***Nickel-based batteries*: The two most popular are NiCd (nickel cadmium) and NiMH (nickel metal hydride). Nickel cadmium can provide a high drain rate, which makes it the incumbent technology in power hand tools. For example, a power drill pulls a large current to provide sufficient torque. However, due to cadmium's toxicity, manufacturers are phasing out nickel cadmium when possible because of ROHS (reduction-of-hazardous-substances) requirements. NiMH is popular in low-cost systems, such as cordless phones. Advances in high-drain capabilities, as well as low cost, mean that lithium ion is moving into both NiCd and NiMH territories.**

***Cell*: A cell is a battery used only in battery packs. The most popular lithium-ion cell is the 18650, an 18-mm-diameter, 65-mm-long cylinder (Figure A).**

Figure A The most popular lithium-ion cell is the 18650, an 18-mm-diameter, 65-mm-long cylinder.

***Battery pack*: A battery pack is a set of cells and their protection/authentication/security circuitry (Figure B). Most lithium-ion rechargeable batteries are battery packs containing one cell, such as those in cell phones, or as many as four cells, such as those in laptops. Battery packs are more than just convenient ways of matching and packaging cells: The requirements for lithium-ion-safety specifications are such that the pack is necessary to package safety circuits into the device. Even a device requiring only a single lithium-ion cell uses a single-cell pack, with the security circuits around the cell, and the whole unit shrink-wrapped or encased in plastic. A single-cell battery pack, such as the one in a cell phone, requires 7 to 8W; a four-cell pack in a laptop requires 35 to 70W.**

Figure B Battery packs package lithium-ion cells and any authentication circuitry into a sealed unit.

***Charge cycle*: Most lithium-ion batteries are fast-charged to 80% of their capacity and then trickle-charged to full capacity. One charge cycle uses all of a battery's power but not necessarily from a single charge. For example, if a device discharges to half its power and then fully recharges, and it repeats this cycle the next day, it would count as one charge cycle. Each time a charge cycle completes, the battery's capacity diminishes slightly.**

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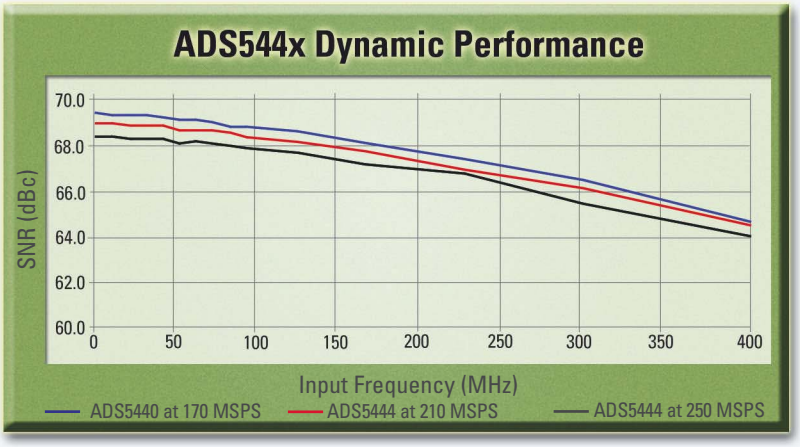
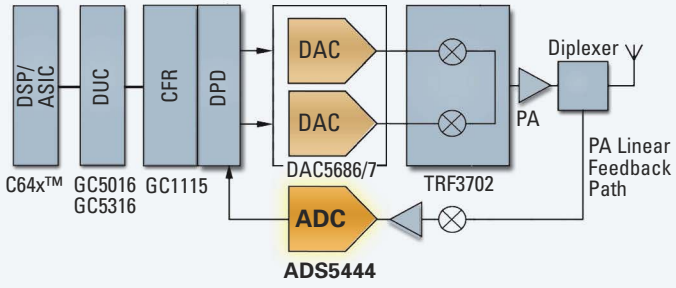


Sample Application: Wideband, High IF DPD Feedback Receiver



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ADS5500	14	125	69.5 at 100 MHz IF	82 at 100 MHz IF
ADS5424	14	105	74 at 50 MHz IF	93 at 50 MHz IF
ADS5541	14	105	71 at 100 MHz IF	86 at 100 MHz IF
ADS5423	14	80	74 at 50 MHz IF	94 at 50 MHz IF
ADS5520	12	125	68.7 at 100 MHz IF	82 at 100 MHz IF
ADS5521	12	105	69 at 100 MHz IF	86 at 100 MHz IF

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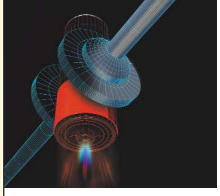

Tichy agrees. "Once the new formulations, such as NCM, start to become available, we're likely to see variations among all vendors," she says. "Variations in cathode formulations may yield differences between vendors' offerings: There may be a slightly different voltage depending on the exact mixture of each vendor." Each manufacturer will designate its cell's operating voltage and give customers the curve they can expect. But, if the pack vendors design a pack for one supplier's cell, it may not be able to get a second source for the new formulation.

Heacock lists useful information available from smart-battery packs with authentication capability, such as cell-ID number, overvoltage rating, temperature reporting, and remaining capacity. He points out that this information becomes important when system designers struggle to make one system work for a variety of users. "Batteries act differently depending on their environment," he says. "For example, an MP3 player in an air-conditioned office experiences different battery response from a player that is left in a car during the summer months. The difference in performance may upset the user who may blame the unit's battery. But if you can design the battery system to allow for the differences in how consumers use them, the batteries seem to be acting the same."

In addition to allowing for system environments and the effect they have on battery performance, designers have to assume that an end customer may use an inappropriate battery pack in a quest to economize on a replacement or backup pack. Gene Armstrong, managing director of thermal and battery management for Maxim, describes a likely scenario: "We have customers who are planning on switching over to the new cells with higher charge voltage of 4.4V, but this change can cause problems from a safety standpoint, because the minute they switch over [to the new cells], there will be a clone battery pack available from some unknown source, using cells with the old technology that charges at 4.2V. If the charging system applies the 4.4V to the old cells, it's potentially a dangerous situation." Authentication devices in the pack can prevent charging circuitry from applying an overvoltage to an after-market clone pack.

Most lithium-ion-battery packs go into laptops and cell phones. According to Tiax's Barnett, these two applications consume more than 80% of lithium-ion-cell sales. However, yet another new cathode formulation is evolving that will make lithium ion practical for high-current applications, such as rechargeable portable power tools, which nickel-cadmium technology currently dominates. $LiMn_2O_4$ (lithium-manganese-oxide) technology has the potential to reach 300A for short pulses of a second or two. (The typical lithium 18650 cell today can support a 4 to 6A pulse.) The new cell can extend 80A for about 10 seconds. Currently, nickel cadmium is the incumbent technology for power tools because of its ability to support a high drain rate. However, nickel-cadmium batteries run afoul of ROHS (reduction-of-hazardous-substances) and WEEE (waste-from-electrical-and-electronics-equipment) legislation, so look to the new lithium formulation of lithium manganese oxide to gradually replace nickel cadmium in power tools. EDN

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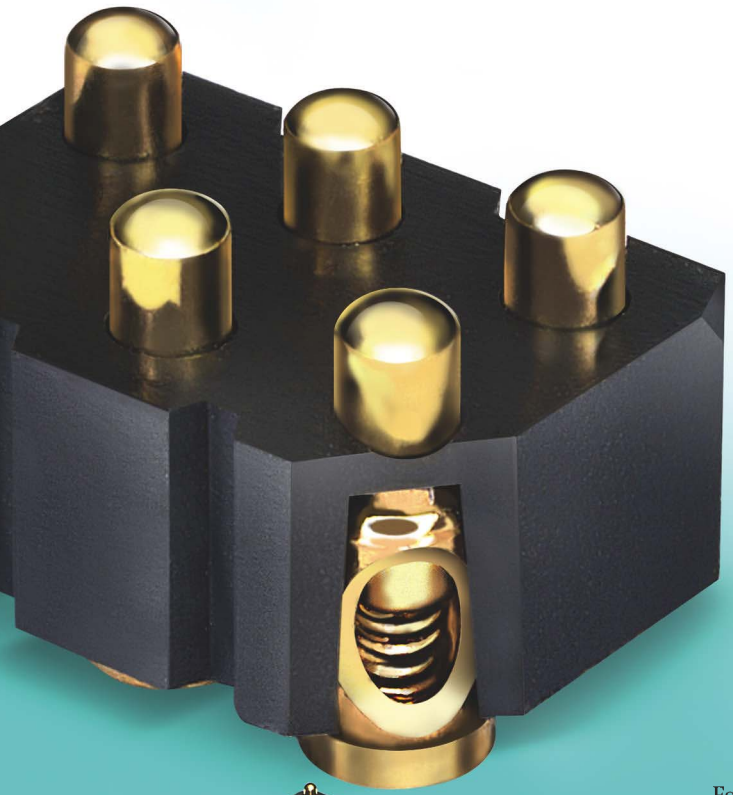

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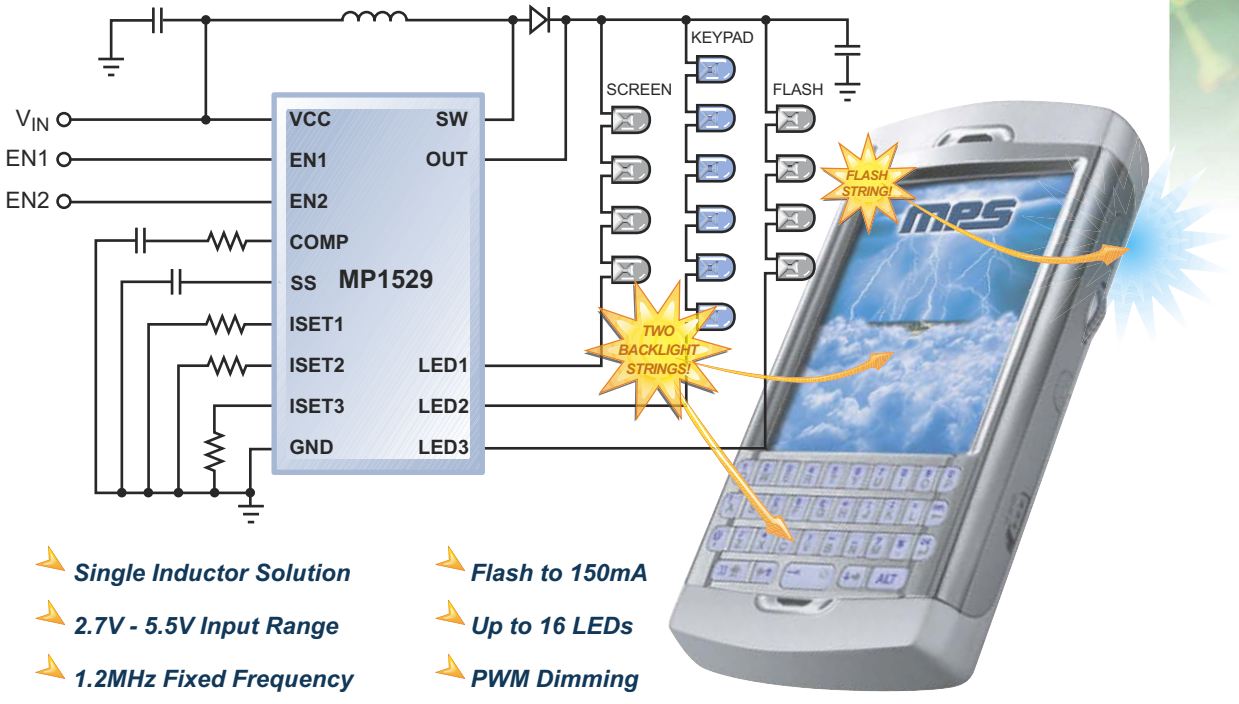

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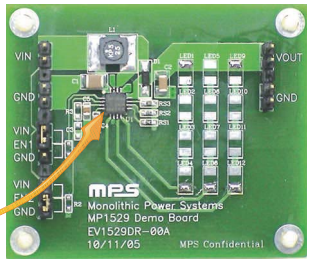

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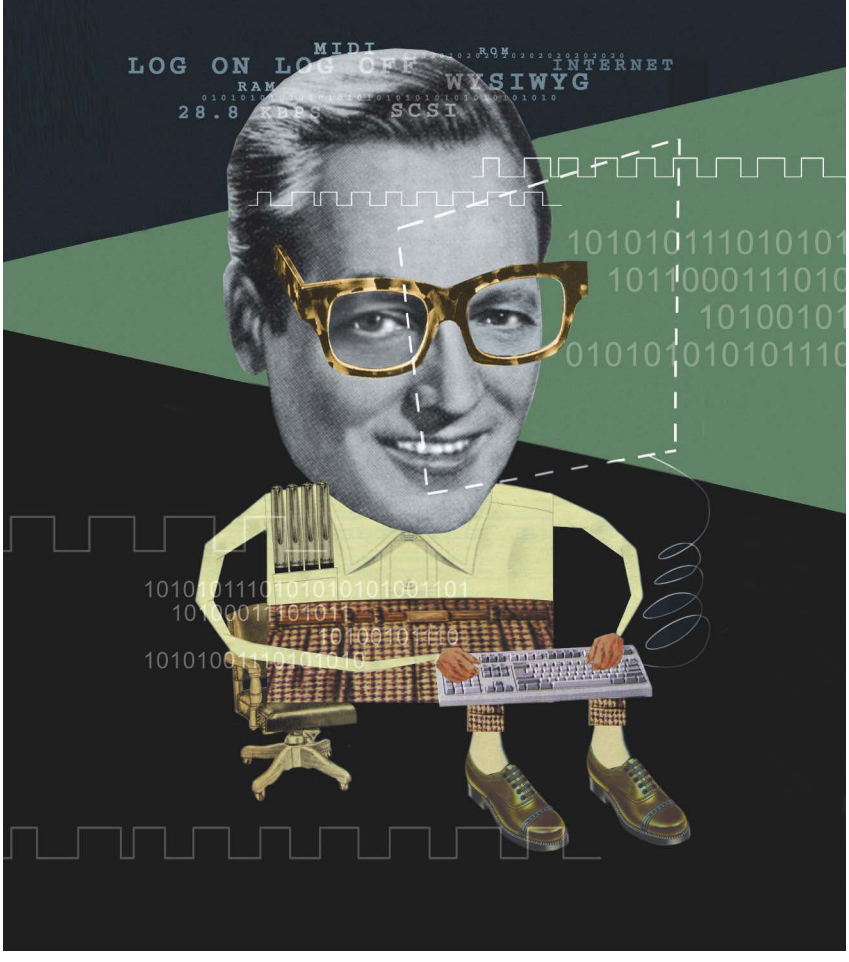

BY JON TITUS • CONTRIBUTING EDITOR

HANDS-ON REVIEW:

ANALYZERS REVEAL DIGITAL SECRETS

PC-BASED LOGIC ANALYZERS CAN REVEAL MUCH ABOUT DIGITAL SIGNALS. HERE'S THE LOWDOWN ON SEVEN MODELS WE TESTED.

Logic analyzers capture digital signals and display state information, timing information, or both. When testing or troubleshooting electronic equipment, engineers use these instruments to extract microcontroller timing information, monitor sequences of digital events, watch instructions go to and from a microprocessor, and so on. Wherever you need to monitor sequences of bits and bytes, you'll find that a logic analyzer fills the bill. In addition to watching the usual flow of signals on parallel lines, some logic analyzers can decode I^2C, SPI, CAN (controller-area-network), and other serial protocols. And, if you plan to debug an embedded computer, you also can decode instructions so that you can watch the flow of a program, step by step, as op-code abbreviations go by on a screen.

Logic analyzers traditionally fit into large desktop enclosures, but several manufacturers now offer small, "pocket-sized" logic analyzers that rely on a host PC for display, control, and storage capabilities. We tested seven of these instruments and report our results for you here. Tests involved the use of a standard microcontroller-development kit and simple programs written in C.

There are several areas of concern to keep in mind while evaluating these or similar instruments in your lab.

Connections: Several analyzers come with small grabber clips. Connecting to eight signals on a row of pins spaced at 0.10-in. intervals provides a challenge. Other instruments provide a choice of female contacts that push onto 0.025-in.[2] pins.

Triggers: All logic analyzers in this review provide triggering, because that's what logic analysis is all about: You want to see what happens when an event occurs. Unfortunately, some analyzers provide triggers that act on only logic levels and, in one case, could set up a trigger based on only four signals. These days, analyzers need level and edge triggering, and some engineers need sequential triggers, such as "trigger if Condition A follows Condition B." Know your triggering requirements, so that a purchase doesn't disappoint you.

Cursors: These movable marks that locate signal features prove troublesome in many displays. Software should give you complete control over cursors and should show you where the cursors are, how to control them, and the time mark they represent in a display. The ability to calculate the time between sets of cursors makes them particularly valuable. A display should not "lose" cursors so that you have to go and look for them.

And last, you cannot have a good logic analyzer without solid documentation.

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For details on our testing tools and procedures, see the sidebar "How we ran the tests" at www.edn.com/051205df1. At this link, you'll also find the code we used for tests 1 and 2, which you will read about in the following pages, as well as a table summarizing each of the seven logic analyzers.

BitScope BS-50 Pocket Analyzer

Price: $345

www.bitscope.com

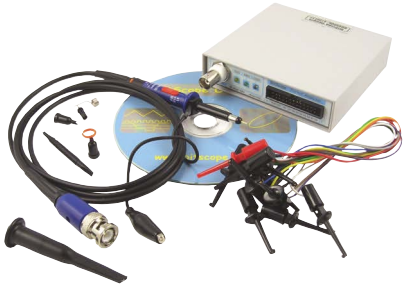
This small module provides logic-analyzer and DSO (digital-storage-oscilloscope) functions, and it includes a single-channel AWG (arbitrary waveform generator). Setup went smoothly, although engineers may find it easier to work with a 26-pin header than with individual wires. The color-coded wires that accompany the analyzer provide a grabber on one end and a 0.025-in. female connector on the other. The grabbers crowd the I/O pins on our test board, but they fit snuggly and held in place during testing.

The BitScope DSO 1.2 software starts easily, but it takes a moment to realize that you have to click the power button to "start" the instrument. The software's initial screen looks like a DSO, but a click on the logic button on the right-hand menu produces the eight logic signals the module can acquire. When the software changes to logic-analyzer mode, the upper-left trigger area displays each logic signal and an associated button that lets you select a logic-zero, logic-one, or don't-care condition for triggering. The software does not provide for edge triggering or for a sequence of events that trigger acquisition of signals.

We ran the Test 1 code on the Rabbit board and set triggering for a logic-one on D0 and a logic-zero on D1. The display seems upside-down, with D7 at the top and D0 at the bottom. The software provides no way to change the color or to name the traces.

To acquire data, users click "repeat" to continuously acquire and display data whenever the analyzer "sees" the trigger condition and is not busy acquiring data. A click on a trace, though, initiates a one-shot capture. The timebase controls let users select a timebase of 25 nsec to 200 µsec and a zoom factor of 10 to 20×. The display shows a time-delay value, the timebase value, and the sample rate. We chose a 1-µsec timebase and a 1× zoom factor, and the data generated by Test 1 appeared in the display area. Although the display triggers properly, we could not relate the TD value to anything we had set or could control.

The display provides an x-axis cursor and a display of the x cursor's time relative to the trigger. But good luck if you can't remember where you placed the cursor the last time you used it. No subdisplay shows the location of the cursor relative to your current view of the acquired data. And you can't click within a display of data to retrieve the x cursor from a distant or forgotten position; you must hunt for it.



We performed the BIOS interrupt-timing measurements on the Pocket Analyzer's data and calculated an average period of 488 µsec. EDN

Bottom line: Before you use this analyzer, the manufacturer should upgrade its software. The inability to easily move a timing cursor and the lack of signal-name assignments and color codes make the instrument difficult to use. Because the manual concentrates on DSO measurements, logic-analyzer operations get scant coverage.

Cwav USBee ZX Test Pod

Price: $895

www.usbee.com

This module provides eight digital inputs, a ground line, an external trigger, and clock lines. The built-in wires come with female adapters that slide onto 0.025-in.^{2} pins. The unit includes microclips that can grab component leads. Sampling of digital signals takes place at nine rates from 1M to 24M samples/sec. Because the module uses a PC's internal memory for storage, acquisitions can run from 1M to 810M samples, depending on the PC memory available. Users can add modules to acquire data from more than eight signals at a time. Each module provides both 5 and 3.3V outputs.

The display window shows all eight color-coded signals, which users can name as they like. Four columns near the signal names let you select sequential-trigger conditions based on logic-one, logic-zero, or don't-care states. If you do not set a trigger condition, the module starts to acquire data as soon as you click on the "acquire" button in the acquisition area. The trigger levels prove easy to manipulate and the module easily acquires data from the Test 1 and Test 2 program runs.

The display area includes two cursors, X and O, that you can move freely through the data. Three windows show the time position of the cursors, as well as the time difference between X and O. You can set X, O, or T (the trigger condition) as the reference for time measurements. Measuring the times between the expected glitch in the data during Test 1 provides an average time of 485 µsec from eight consecutive measurements. The cursors and the display con-

trols are easy to use. An additional measurement, Insta-measure, lets you select width, frequency, period, or byte. Select one of these measurements, and it appears next to the cursor as you move it among the waveforms.

Because the module comes with what looks like an external trigger input, we decided to use it to trigger the logic analyzer. Although the USBee ZX software includes help files that exist as video segments, the triggering options that the video segment describes do not match the latest version of the logic-analyzer software. A printed manual would help.

How hard can it be to configure a simple trigger input line? We set up conditions to try and clicked on the "acquire" button. A blue "waiting-for-trigger" indicator flashed for longer than appropriate for the signal we had selected as the trigger source. So, we clicked on the "stop" button to abort the run. That action sent the software into the "not-responding" condition, and, in this state, the Windows task manager could not shut down the program. To double-check the operation, we tried similar external trigger actions, and all locked up the program. If you leave it long enough, the program eventually shuts down.

Tim Harvey at USBee at first remarked that we had uncovered an unknown bug in the software, which should otherwise let users gracefully "back out" of a condition in which the software waits for a trigger and a clock signal. He later explained that we probably needed to upgrade our USB-port drivers because early drivers had a problem that prevented certain timing operations from working properly. EDN

Bottom line: The logic-analyzer functions work well, and the ability to cascade USBee ZX modules in parallel makes the logic-analyzer functions useful. This unit will appeal to designers who develop small embedded systems and who need basic logic-analyzer functions.

Dynon Instruments Elab-080

Price: $495

www.dynoninstruments.com

The Dynon Instruments Elab-080 provides a 16-channel logic analyzer, a two-channel digital oscilloscope, and a one-channel arbitrary- waveform generator. The package includes two 60-MHz 1×/10× scope probes. We confined investigations to the logic-analyzer portion of the unit and its software. The package includes the main instrument box, a large plug-in power supply, and connection leads. The leads connect to a header that furnishes eight signal leads and a ground for each. Labels CH1, CH2, and so on mark the leads so that you need not rely solely on the color-coded wires for identification at your system under test.

Unfortunately, the package lacks a CD-ROM, manual, and quick-start guide. Instead, a slip of paper asks users to visit the Dynon Web site to download the latest software. We downloaded the software onto a USB memory stick and moved it to an isolated lab PC. The setup went well, and the installed software displayed windows for the logic-analyzer waveforms, oscilloscope signals, and spectrum display.

Controls make it easy to set a sample rate (1 kHz to 100 MHz in one, two, or five steps) and a sample size (1k sample to 32k samples in 2n steps). To test the logic-analyzer functions, we ran Test 1 so that we had some data to capture. Clicking a green arrow button in the control window started an acquisition, but we could see no changes in the data, and, no matter how we adjusted the sample rate, the display timing remained fixed.

Off to one corner, the control window displays a group of two buttons: (DSO/LA Zoom). Yes, the label is in parentheses. The buttons carry labels S and nS. Clicking the buttons zooms the display out and in, respectively, so we could see more or less of the data. After zooming appropriately, we could see the eight logic-zero signals.

Clicking on the logic-analyzer tab in the control window opens a subwindow that lets you quickly label signals, designate a signal's source, and change a signal's displayed color. Changing a name does not change the signal's channel number—a nice feature that makes it easy to name signals and still know what points they come from on a circuit. A "buses" tab lets users group signals and display bus information in octal, binary, decimal, or hex format.

A "trigger" tab lets you select an optional trigger, but trigger choices appear limited. You can select to trigger only on patterns that involved channels 00 to 03. The trigger-setting window accepts any binary pattern except for 00002. The unit's help file explains that a hard-

ware limitation causes that problem. The analyzer may accept an external trigger signal on a separate pin, but nothing in the trigger window provides a clue about using this input line. Several trigger combinations work as you would expect. When you remove the check mark from the enable-trigger option, the analyzer simply acquires data as soon as you click on the green arrow button.

The display provides two timing cursors, A and B, that have little value.

The Elab-080 software displays numeric-timing information in a separate window so that you can view state changes as they relate to sample times (timing analysis). Unfortunately, the display simultaneously shows only 19 time-stamped samples, and you cannot expand the size of this window.

The lack of a manual and a quick-start

guide troubles us. A user new to logic analyzers and other PC-based instruments needs some hand-holding that this product doesn't provide. The software comes with a help file that includes some explanations of controls and displays, but the information about the timing cursors, for example, simply explains that they exist and that a user can move them.EDN

Bottom line: The instrument provides more functions than you would expect, which may make it attractive in some lab situations. The lack of triggering options and cursor-timing information, however, limits the use of this instrument as a logic analyzer. When compared with the other instruments, this one fails to deliver the performance you should expect from an instrument that costs almost $500.

Link Instruments LA-2124-128K

Price: $800

www.linkinstruments.com

Link Instruments provides a family of logic analyzers that operate with a PC over either a parallel-port or a USB-port connection. We chose the least-expensive model, which uses the parallel port. Users who have another device connected through the parallel port may opt for a USB-compatible model with a faster sampling rate and more channels but at higher cost. The software setup goes quickly until Windows asks you to install a device driver. The company's technical-support person claims that the driver exists within the installed software directory (C:/la2124), not on the supplied CD-ROM. He also suggests downloading Version 1.34 of the software.

Hardware setup goes easily, too, although we dislike pushing individual wires onto small pins. We'd prefer a cable connected to a single header. The analyzer comes with 30 color-coded E-Z-Hook (www.e-z-hook.com) clips, though, so you can attach the clips to the signal pins and the clips to the analyzer's wires. This model accommodates as many as 24 logic inputs, and it provides for an external clock and trigger signal.

After connecting eight wires plus ground, we ran the LA-2124 software and set up Test 1 on the Rabbit test board. A click on the displayed "go" button causes the unit to acquire data in single, normal, or automatic mode. In single or normal mode, the analyzer waits for a trigger and then acquires data. Normal operation acquires a new buffer's worth of data after each trigger. Automatic mode acquires data regardless of the trigger settings.

After adjusting the sample rate with a plus and a minus button, we could see useful test results. (The sample-rate control offers 14 1-2-5 steps from 5k samples/sec to 100M samples/sec.) A right click on the signal-name column lets you change the designation for each signal and its color. Trigger setup involves clicking on "trigger" and then on "trigger word." You can set up a pattern of logic levels and don't-care conditions (logic zero or logic one) for a group of eight signals. You can select a trigger or trigger-false condition, and the software lets you establish triggers in binary, hexadecimal, ASCII, or decimal formats. The trigger menu also provides a threshold setting that ranges from −1.15V to +2.80V. The default is 1.4V.

Set the relative size of the pretrigger and post-trigger record lengths by dragging the red trigger cursor along a time line that represents the data-buffer's depth. A small box, or timing window, on this line represents the amount of information in the display window below it. Cursors A through D let you mark positions in the data, and you can use cursors A and B to measure the time between two points or between each cursor and the trigger point. The BIOS interrupt period is 488 μsec.

The cursors are easy to use and helpful. You can track a cursor by its color, and a check mark in a small display also lets you know which cursor you have under control of the mouse. Cursor movements involve "grabbing" one with the mouse, or you can select one in the upper-left cursor box and use six buttons to move it left or right in time increments. The cursors also appear along the time line, so you always know their locations. Menu choices let you quickly move the cursors into the display area. The display produces the state data as hexadecimal, binary, decimal, or ASCII characters. You can assign your own values to the display and can include a translation table. The translation table lets you establish op-codes for

a processor so you can examine instructions and data as they flow over buses in a system. By adding extra columns of data in different formats, you can examine state information as binary and hexadecimal codes.

The software neither "collapses" a group of signals into a bus nor displays a hex, decimal, or other code for bused signals. But the state window provides some of those capabilities. The state window and the timing window do not link to each other, although you can coordinate cursors between them. You can insert a "spacer"—essentially, a colored bar—between groups of signals to separate them from other signals.EDN

Bottom line: There's a lot to like about this instrument. The built-in ability to handle 24 inputs as well as an external clock and trigger makes this instrument useful for embedded-system designers. The ability to add modules makes it easy to expand digital inputs. The menus are generally intuitive, although we had to ask tech support how to remove a spacer. If the analyzer lacks anything, it's the ability to set up edges as triggers and to establish sequential trigger conditions. We give this unit high marks, and, in this case, the lack of a printed manual causes no problems.

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NCI GoLogic-72 System

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The GoLogic-72 System provides for as many as 72 digital inputs and eight clock inputs, which makes it a powerful tool for testing and debugging embedded systems that require monitoring of several buses, I/O ports, and control signals. The unit comes with all 72 connections, split into two groups. Each group of eight labeled connections passes through a small harness that makes it easy to handle them all simultaneously. This feature simplifies setup when attaching connections to a board. The wires each furnish a female connector that pushes onto 0.025-in.^{2} pins, which is how we used the logic analyzer. NCI also provides micro-grippers ($4 each) and nano-grippers ($7 each) to connect with small and tiny component leads.

The GoLogic system comes with a CD-ROM, and it takes little time to install the software and get it running. The module connects to a supplied power cube and to a PC through a USB cable. The comprehensive manual provides basic information on how the analyzer works and then goes into details about sampling, clocking, state analysis, timing analysis, and triggering. Unfortunately, the manual looks formidable, and no quick-start tutorial exists to take you on a tour through the many options and menus.

Lacking such a tutorial, we plunged in and connected the lines labeled A0 to A7 plus two ground lines to the test board. A setup menu lets you select a sample rate, memory depth, and the type of sampling. Nine options for sampling include I^{2}C and SPI modes for troubleshooting serial communications in embedded systems.

Next, you select the channel groups, which show the wire color codes and indicate signal activity on lines A0 to A7. The threshold for the signals is 1.58V, but you can reset it for ECL signals or adjust it from −4.90 to +5.27V for other logic families.

We downloaded Test 1 to the Rabbit test board to make information available to the analyzer. If you need to perform more than basic triggering, plan to spend time learning about the various triggering modes by experimenting with them. To start acquisition of data for Test 1, we wanted to trigger on a falling edge on signal A0. Clicking on the setup tab lets you select a simple edge trigger, but we couldn't figure out how to select the A0 signal. After we gave up and switched back to the waveforms display, we noticed small, gray squares associated with each signal. Clicking on these squares lets you select

a rising, falling, rising-or-falling, or unused triggering attribute. You can scan through the trigger settings you used previously, which makes it easy to keep several settings at hand for complex tests.

Displays that include at least one channel (signal) include three pairs of cursors you can move with the left or the right mouse button to measure times between events. Luckily, you need not drag a cursor from place to place. Clicking on an area of the waveform display moves the selected cursor to the clicked-on position. The cursor notations need some enhancements, though. It is difficult to tell which set of cursors is active and which mouse button controls a given cursor.

Moving on to the binary-count test (Test 2) lets you set up a pattern trigger for FF (hexadecimal) and set the duration of the trigger for at least 8 µsec, which put it about in the middle of a 1-LSB level. That trigger setup works, and the display provides the expected data. In this test, the gray trigger squares indicate logic levels rather than transitions. You can click on these squares to change trigger conditions without going back to the setup menu.

The logic-analyzer software also provides a sample-by-sample numeric display of information. So, the software lets you monitor data value on a bus rather than waveforms. You can still use the cursors to mark values and determine the time between them. If you have a waveform and a numeric display open simultaneously, moving around in one display also moves your view in the other. Thus, you can easily track logic levels and numeric data. The logic analyzer detects the anomaly that the Rabbit board's BIOS causes and measures the time over 10 occurrences over a period of 489 µsec. The display also shows two "glitches" on the A7 and A6 lines where the other signals change state. The period of these glitches always equals the sampling period: 8 nsec at 125M samples/sec and 20 nsec at 50 MHz. So, it seems unlikely that the glitches existed; they do not expand and shrink in sync with the sampling clock. But glitches might arise from simultaneously switching so many loads (the LEDs).

Do the glitches you observe with the logic analyzer but not with the scope exist, or does the logic analyzer "see" something that doesn't exist? You'd need a storage scope to tell. EDN

Bottom line: Although priced much higher than any other analyzer, the wealth of triggering options provides a strong justification for buying this unit. The display options and the cursors make it a solid analytical tool. Plan to spend time learning about the triggering modes and options. Unfortunately, lack of time prevented us from exercising many capabilities, such as searching data for patterns and triggering a storage scope and simultaneously displaying analog and digital data. The analyzer links with disassemblers and displays C/C++ source code so you can observe op-code-by-op-code operation of a program. Software add-ins that provide these functions cost extra.

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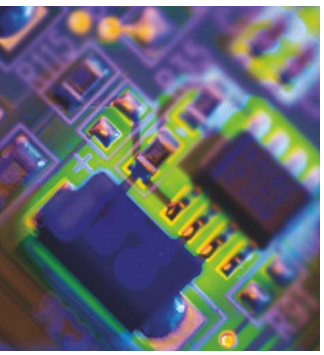

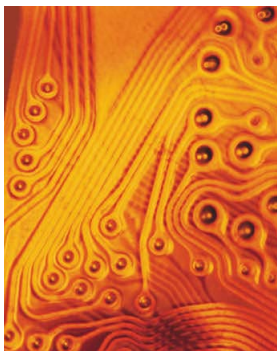

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www.cirrus.com/CS42L51

Saelig Ant16 USB Logic Analyzer

Price: $333;
16-channel clip-lead set and cable, $39

www.saelig.com

The Ant16 analyzer comes with an analyzer module, clip-lead set, getting-started guide, and mini-CD-ROM. The equipment provides a basic logic-analyzer module and software that communicate through a USB connection. Software setup takes little time, although Windows XP displays a caution message about using software that had not passed "Windows Logo" testing. We ignored the message and proceeded to start the logic-analyzer software. The unit provides sample steps in 21 increments, from 100 Hz to 500 MHz, plus a synchronous mode controlled by an external clock input.

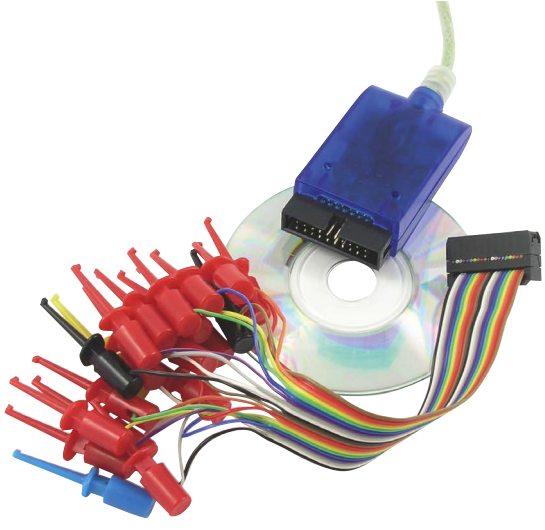
Setup with the test board takes little time, although placing eight signal clips and two ground clips on a row of 0.025-in. header pins makes for a crowded space. Users may want to make up their own color-coded cables with smaller clips from a supplier such as E-Z-Hook (www.e-z-hook.com). Test leads that push directly onto square pins would help, too.

After you connect the analyzer and the test board and start the Ant16 software, a small display indicates signal activity on all the inputs you connect. This feature indicates that the module "sees" activity on its connections.

The logic analyzer has no difficulty displaying the results of a standard test, although figuring out the triggering modes causes some head-scratching. The manual's academic descriptions of how trigger conditions work provide no hands-on explanations of how to make the triggers work. Without screenshots, references to menus, and step-by-step instructions about using triggers, the manual has little value, and it diminishes the value of this product.

Triggering involves setting levels, signal edges, and don't-care conditions for the signals in use near each displayed signal. Once you figure out how to set a simple trigger condition to match a pattern or detect a signal change, you'll have no difficulty capturing data. A slider on top of the display lets users set the pretrigger record from 10 to 90% of the display in 10% increments.

Don't expect the Ant16 to operate like an analog scope, though. The display doesn't refresh until the software detects a trigger condition and acquires all the data. You might expect to see a constant flow of digital information when the unit is in continuous mode, but the software instead constantly updates the entire display after each trigger. It takes a bit of getting used to.



Although the cable provides a connection for an external trigger signal or clock input, the manual lacks information about how to set up and use this line. Likewise, a separate output line, trigger out, may serve a useful purpose, but no documentation describes it.

The display provides a cursor that shows the hexadecimal and decimal value for an eight-input group of signals. We found no way, though, to change the display to octal or to group other signals and display their numeric value. The display also includes two cursors (red and blue). The red one moves, but the blue remains fixed. The manual dismisses these cursors with one unhelpful sentence. Clicking on the logic signals moves the red cursor and provides timing information, which is helpful. The purpose of the blue cursor remains unknown.

While running the high-speed binary-counter program (Test 2), the display shows the expected odd timing patterns. You use the red cursor to extract the time stamps for the observed "glitches," although you have to subtract sequential values to get time differences. Positioning two user-controlled cursors to compute a time difference would have sped the process. After measuring seven periods between glitches and averaging them, we came up with a 488-μsec period between them. That value matches the period expected from the test board. EDN

Bottom line: Although this analyzer's logic-signal capture works well, we cannot recommend it until the manufacturer revises its manual to include how-to information and examples that show specific settings and operations. The software may provide many capabilities beyond those we discovered, but who knows? And we'd still like to know what the blue cursor does.

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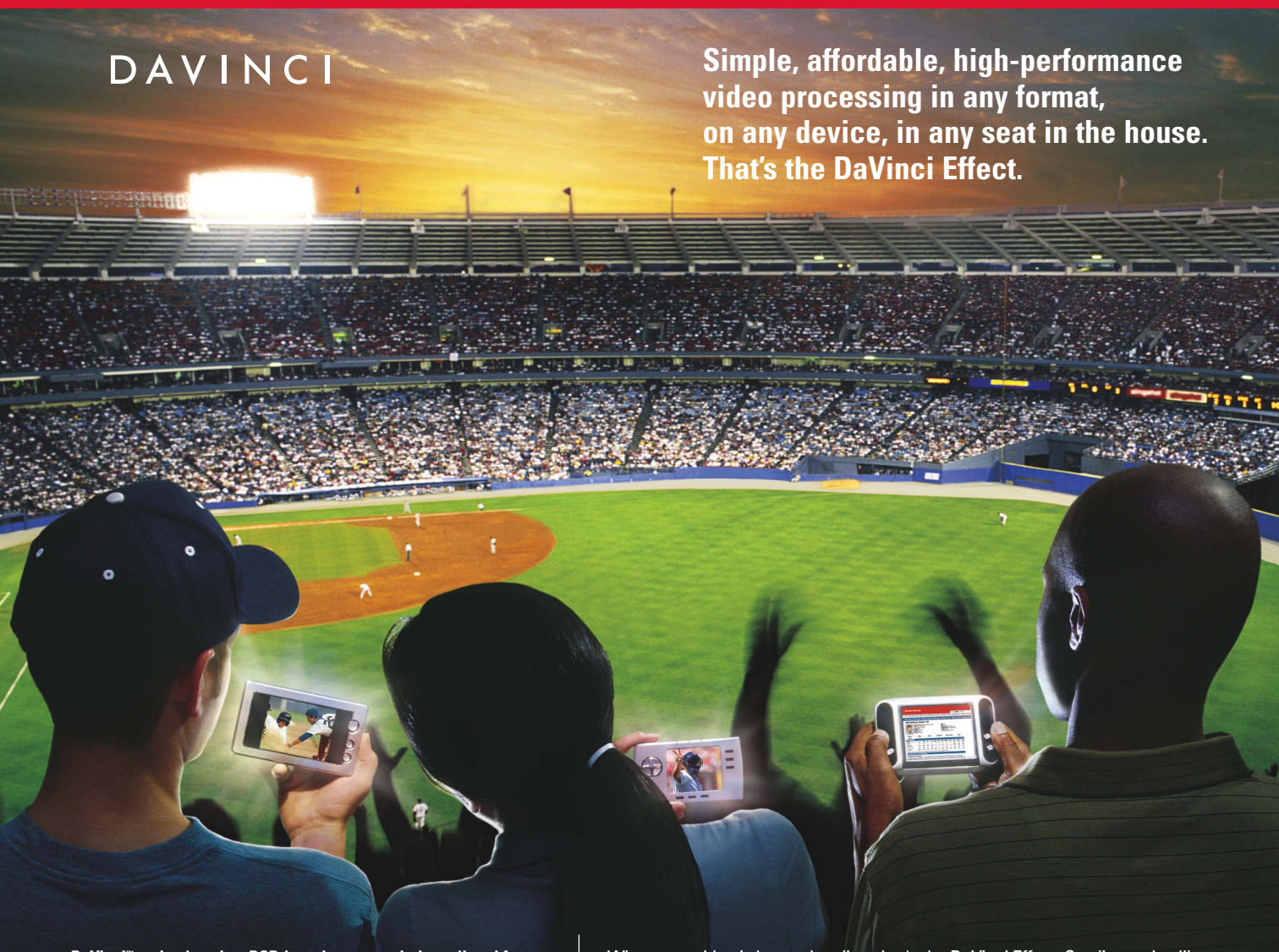

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Price: $499

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Although the software setup instructions don't follow the printed user's guide, poking through menus leads you to the right choices: CDWeb→More Links: Software→d_dv1. The program starts the installation of the DigiView code. Connection of the module through a USB cable and installation of the DigiView driver went flawlessly, though.

The small logic-analyzer module simplifies connections by providing access to 18 input channels and two ground signals through color-coded wires. Each wire comes with a female adapter that connects directly with 0.025-in.^{2} pins like those on our test board. The DigiView package includes small clips, too, so users can grab component leads.

As the code starts, it produces a colorful display of sample information on which you can try operations. But why take the simple path? We guessed and clicked on Config, which popped open a window that lets you select signals by their color-coded wires, assign them a name, choose polarity (invert the displayed logic level), and designate the displayed signal's color. In addition, you can easily group the eight test signals to form a bus.

The Config menu also assigns trigger conditions—combinations of logic levels on input lines followed by the detection of signal edges. This type of trigger is not as sophisticated as it is on other analyzers, but, for many situations, it does nicely. We set up several trigger conditions for the eight inputs.

After you choose and arrange your signals, you turn to the display, which presents signals in a clean and colorful format. Two waveform displays show the same information at different zoom levels.

Running the DigiView logic analyzer requires only a click on the Run button. The module acquires data at a fixed 100M-sample/sec (10-nsec) rate. Unlike other analyzers that store information, the DigiView saves data in compressed form, the equivalent of a 90-Gbyte file, according to the company. The software uncompresses only the data a user wants to examine on the PC's display. If the module sees no changes on its inputs, it doesn't save anything. Thus, when signals do not change rapidly, the "length" of the saved data record expands. So, if you need to monitor sequences of infrequent changes, this unit fills the bill.

After acquiring data from the test board, we "unlinked" the two displays so that we could independently investigate the digital information. Linking the signals, though, lets you home in on an area of interest and then zoom in on it in the other display. Because we defined a bus that combines the eight values, they appear as one logic trace with superimposed hexadecimal values, as space permits. Bus traces include a small plus sign, which, when you click on it, expands the display to show individual bus signals.

The DigiView software also includes a sophisticated search feature that lets users find conditions, such as signals at a specified level, times above or below a limit, and so on. When the software finds a condition, it can attach a cursor mark to it. Search criteria you plan to use often can reside in the search-manager window. The software comes with several examples that show how to apply a search.

The display includes six cursors—A, B, C, D, X, and Y—that you can move along traces to indicate events and measure relative times. The display notes the period between cursors, which makes them handy for determining the times between events. Because the cursor can "stick" to a given trace, you can easily measure times between events on different signals. Cursors also "snap" to signal transitions.

The display of Test 2 data shows the timing anomaly you would expect due to the regular interrupt from the real-time clock on the Rabbit processor board. Placing the X and Y cursors at the start of two "glitches" shows a period of 489 µsec. EDN

Bottom line: This excellent small logic analyzer offers sophisticated display and analysis options. It is easy to set up and use. We recommend it to anyone involved with analyzing logic signals in an embedded system. This unit provides a fixed 1.6V threshold, which makes it suitable for logic families that operate at 2 to 5V logic levels. It is a solid value for the money.

This article originally appeared in EDN's *sister publication,* Design News *(www.designnews.com).*

Analog Applications Journal

BRIEF

Li-Ion Switching Charger Integrates Power FETs

By Anne Huang • Marketing Manager

1. Introduction

Linear battery chargers suffer from excessive power dissipation when the input-to-output overhead voltage and/or charging current are high. Take the example of a typical portable DVD player configuration which incorporates a 2-cell Li-Ion battery pack, a car adapter at 12V and a charge rate of 1.2A; the power dissipation of a linear charger is above 5W on average. A simple solution to overheating is the bqSWITCHER™ bq241xx series switching charger. The internal power FETs are capable of supplying up to 2A of charging current. The synchronous PWM controller operates at 1.1MHz from an input voltage up to 18V, making it ideal for use in systems powered by 1-, 2-, or 3-cell battery packs. The high-voltage, high-current and high-efficiency features together with integrated reverse leakage protection and internal loop compensation are nicely housed in a small 3.5mm x 4.5mm QFN package, saving board space and reducing system design time.

2. Design Example

Adapter Voltage: 12V
Battery Pack: 2S Li-Ion, 1800mAH
Battery Regulation Voltage: 4.2V/Cell
Battery Cutoff Voltage: 3V/Cell
Fast Charge Current: 1.2A
Pre-charge and Termination Current: 120mA
Safety Timer: 5 hours

2.1 Determine the Inductor L

Given 30% ripple current, the inductance is given by:

$$L1 = \frac{V_{IN} - V_{BAT}}{\Delta I_L}\frac{V_{BAT}}{V_{IN}}\cdot\frac{1}{f_S} = \frac{12-8.4}{30\%\cdot 1.2}\frac{8.4}{12}\cdot\frac{1}{1.1\cdot 10^6} = 6.364\mu H \quad (1)$$

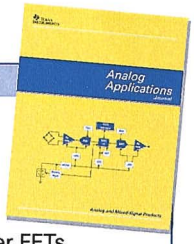
Select L = 8.2µH.

The inductor saturation current should be larger than the peak current to prevent inductor saturation.

$$\Delta I_{L\_MAX} = \frac{V_{IN} - V_{BAT}}{L}\frac{V_{BAT}}{V_{IN}}\cdot\frac{1}{f_S} = \frac{12-6}{6.8\cdot 10^{-6}}\frac{6}{12}\cdot\frac{1}{1.1\cdot 10^6} = 0.40A \quad (2)$$

$$I_{pk} = I + \frac{\Delta I_{L\_MAX}}{2} = 1.2 + \frac{0.40}{2} = 1.4A \quad (3)$$

Select: Sumida CDRH5D28 inductor (8.2µH/1.6A/39mΩ)



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- TLC5940 DOT Correction Compensates for Variations in LED Brightness
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2.2 Determine the Output Capacitor C

The resonant frequency of the internal loop compensation is approximately 16kHz. To achieve optimum loop stability,

$$C = \frac{1}{(2\cdot\pi\cdot f_o)^2 L} = \frac{1}{(2\cdot\pi\cdot 16\cdot 10^3)^2\cdot 8.2\cdot 10^{-6}} = 12\times 10^{-6}(F) \quad (4)$$

Select: 10µF, 25V X7R 1206 ceramic capacitor.

2.3 Determine the Sense Resistor, R_{SNS}

V_{RSNS}: 100mV to 200mV

In order to get a standard resistance value, select V_{RSNS} = 120mV,

$$R_{SNS} = \frac{V_{RSNS}}{I_{BAT}} = \frac{120mV}{1.20A} = 0.1\Omega \quad (5)$$

$$P_{RSNS} = I_{BAT}^2 R_{SNS} = 144mW$$

Select: 1%, 100mΩ /0.25W resistor.

2.4 Determine R_{SET1} and R_{SET2}

V_{ISET1} = 1.0V, V_{ISET2} = 0.1V, K_{SET1} = K_{SET2} = 1000V/A,

$$R_{SET1} = \frac{V_{ISET1}\bullet K_{SET1}}{I_{FAST-CHARGE}\bullet R_{SNS}} = 8.33k\Omega \quad (6)$$

$$R_{SET2} = \frac{V_{ISET2}\bullet K_{SET2}}{I_{PRE-CHARGE}\bullet R_{SNS}} = 8.33k\Omega \quad (7)$$

Select: 1%, 8.33kΩ resistors.

2.5 Determine C_1

C_1 is used to program the fast charge timer.

$$C_1 = \frac{300\ min}{2.6\ min/\ nF} = 0.115\mu F \quad (8)$$

Select: 0.12µF or 0.1µF/X5R or X7R ceramic capacitor for good temperature performance.

2.6 Determine R_{T1} and R_{T2}

R_{TS}, the resistance of the thermistor, normally drops with temperature. Assume using 103AT-2 thermistor, the resistance at cold temperature and hot temperature is: R_{TS_COLD} = 27306Ω (0°C), R_{TS_HOT} = 4935Ω (45°).

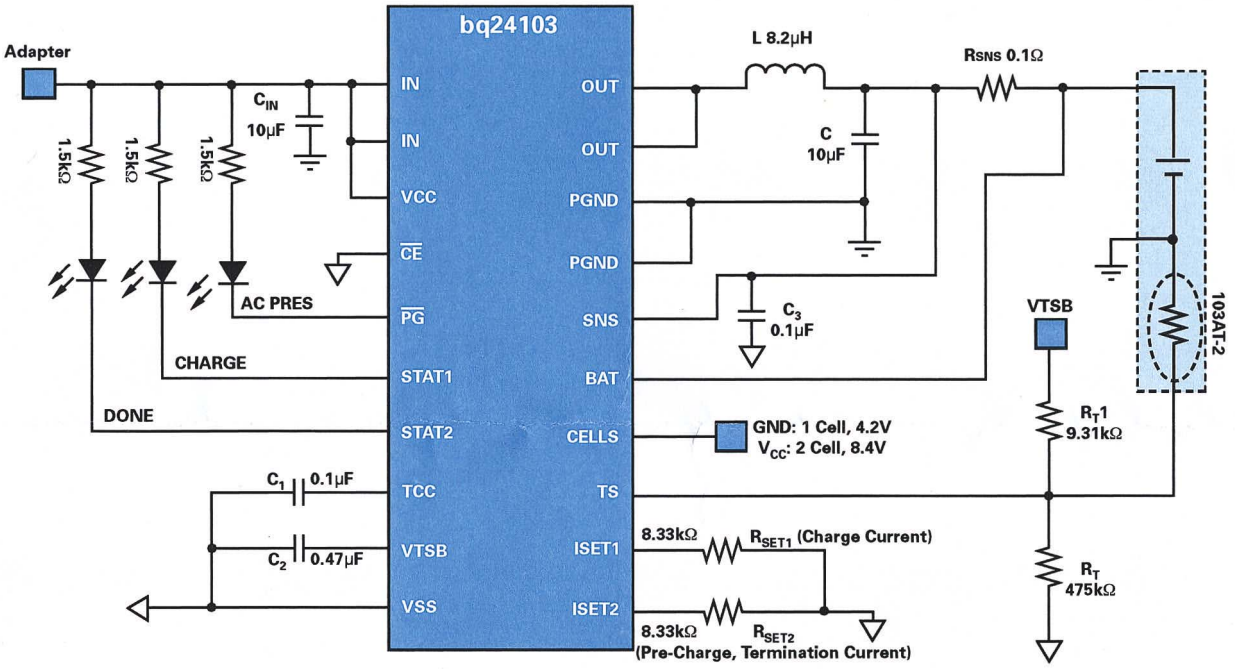
The voltage threshold at cold temperature V_{LTF} = 73.5% • VTSB. The voltage threshold at hot temperature V_{HTF} = 34.4% • VTSB. Therefore:

$$\frac{R_{T2} \,//\, R_{TS\_COLD}}{R_{T1} + R_{T2} \,//\, R_{TS\_COLD}} = 73.5\% \quad (9)$$

$$\frac{R_{T2} \,//\, R_{TS\_HOT}}{R_{T1} + R_{T2} \,//\, R_{TS\_HOT}} = 34.4\% \quad (10)$$

The equations above gives R_{T1} = 9.31kΩ, R_{T2} = 475kΩ

Figure 1: bq24103 Application Circuit

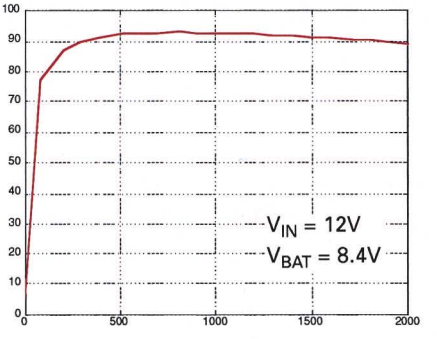


3. PCB Layout Considerations

The measurement of the efficiency using the bq24103 EVM is shown in Figure 2. Below are some layout guidelines to maximize efficiency:

3.1 Make the connections of the power stage as wide and short as possible.
3.2 The ground planes of the power stage and the control stage should run separately, and be connected together at a single point.
3.3 Place the decoupling capacitors close to the pins.
3.4 Minimize the current sensing feedback loop.
3.5 Place the inductor close to the OUT pin.

Figure 2: Efficiency vs. I_{bat} (V_{IN} = 12V, V_{BAT} = 8.4V)



For more information:

Using key word search, download datasheets and other literature at:
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High Side Current Sensing

High Performance Analog Solutions from Linear Technology

One of the most common tasks in analog circuit design is measuring current. A current sense circuit often resides at the heart of power and battery-life management, bias current control, load monitoring, fuse monitoring, fail safe circuitry and instrumentation. The constraints, demands and ever-expanding list of applications constantly push the state of the art in current sensing. This article describes the advantages of high side current sensing, and spotlights new amplifiers for this application.

Measuring on the High Side

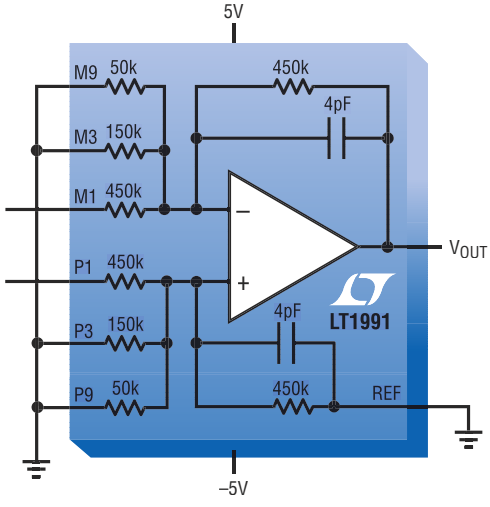
In the ideal circuit, current would be measured without interrupting the current path. For example, one could use a magnetic pickup to sense current, except that magnetic sensors have poor accuracy. As a result, current sense circuits typically place a resistor directly in the current path and use an amplifier to measure the voltage drop across this resistor.

This task might seem trivial until you consider where to place the current sense resistor. Placing the resistor in line with the ground return, known as low side current sensing, presents several challenges. For one, the load no longer has a solid ground connection; as current changes, the relative ground of your circuit changes. A fluctuating "ground" can create signal errors for charging or power management circuitry. Also, in order to accurately measure current, you must completely isolate and contain all current through the sense resistor. Anyone who has struggled with ground loops knows that this can be quite difficult.

To eliminate low side issues, the current sense resistor can be placed between the positive supply and the load, and is referred to as high side current sensing. A high side current sense must discern a small sense voltage on top of a high common-mode voltage.

The Straightforward Approach

One technique for high side current sensing is first to attenuate the current sense signal and then to use a difference amplifier to extract and amplify the differential voltage. A simple resistor divider on the amplifier can be used, as shown in Figure 1. This circuit requires excellent resistor matching and a differential amplifier with a high common mode input voltage and good common mode rejection (CMRR). Linear Technology's LT®1991 difference amplifier provides an outstanding example of this type of circuit, with



Gain=1
Input Common Mode Voltage >±50V!

Figure 1. High Side Current Sensing Using a Precision Difference Amplifier

High Side Current Sensing

built-in resistors that are matched to within 0.01%. In addition to low offset, offset drift and input bias, the LT1991 can accept input voltages up to 60V with a CMRR of 75dB.

Selected Current Sense Amplifiers

Part	LT6100	LTC6101/HV	LT1787/HV
Bidirectional			√
High Voltage (≥ 60V)		√	√
Fast Response (< 10μsec)		√	√
Precision (Vos ≤ 300μV)	√	√	√
Small Footprint (≤ 3x3mm)	√	√	
Micropower (typ ≤ 60μA)	√		√
Gain Configurable	√	√	

Dedicated Current Sense Amplifiers

Using a precision difference amplifier with well-matched resistors works well, although high common mode voltages may provide unacceptable accuracy. Consider measuring 100mV across a sense resistor with an amplifier that has a fixed 1mV offset voltage. This translates to an error of 1 percent. If 100mV is now measured at a high common mode voltage that must be attenuated by a factor of 10, the 100mV signal reaches the amplifier input as 10mV. Accuracy has now been reduced to 10 percent. Accuracy will be further reduced by resistor matching error, and common mode rejection error (CMRR).

Dedicated high side current sense amplifiers are a better choice for high voltage, high side measurements as they are designed to operate at high common mode voltages with excellent precision. Linear Technology offers three families of high side current sense amplifiers to cover a broad range of applications.

Gain Accuracy Matters

For uncompromising designs where performance, size and flexibility are key, consider the LT6100. This high side current sense amplifier includes an output buffer with internal resistors for six gain configurations and 0.5% gain accuracy, all in a 9mm² package. The input of the LT6100 is a robust differential amplifier with a low 300μV offset and the ability to accept fully differential voltages up to 48V. As a result, this part can monitor a fuse or MOSFET without concern for an open circuit and can withstand a –48V reverse input condition. A separate supply input operates from 2.7V to 36V and draws only 60μA. When powered down, the input pins become high-Z, preventing current draw. The LT6100 is a complete, precision solution that's ideal for today's power-conscious and size constrained high performance designs.

Watch Inductive Kick Back

If you're looking to protect your equipment from load faults or high voltage flyback conditions, consider the LTC®6101. As a result of its exceptionally high common mode voltage capability, the LTC6101 can operate throughout high voltage peaks that can result from power supply failures or catastrophic load changes. And with its 1μsec response time, the LTC6101 is ideal for taking control of these situations when used to gate the supply or load. In addition to protection applications, the LTC6101 may be used for high-quality monitoring, as it offers outstanding precision and flexibility in a tiny ThinSOT™ package. Input bias current is 170nA max, input offset voltage is 300μV max, and offset drift is typically 1μV/°C. Gain is selected via 2 resistors and better than 1% gain accuracy is easily achieved using precision resistors. For automotive and industrial applications requiring fast, accurate current measurements, Linear Technology's LTC6101 offers uncompromising performance.

Handling Fault Conditions

When used for power monitoring, current sensing is often the key element for detecting and responding to faults. Inductive elements can wreak havoc on a system, causing large common mode fluctuations. It is important to assess the potential peak voltage amplitude and duration during a fault. As an example, for transients up to 105V, the LTC6101HV will continuously monitor throughout a fault and can initiate a shutdown with its 1μsec response time. On the other hand, when a fault induces large, prolonged differential voltages across the amplifier inputs, the LT6100 is ideal. This part can withstand differential voltages up to the entire common mode range, which could occur when using a fuse or MOSFET as your shunt device.

Bidirectional Operation

For some applications, bidirectional current sensing is required. For example, a battery operated device with both charge and discharge currents might require bidirectional current sensing. One method for achieving this is to combine two unidirectional parts, such as the LTC6101 and LT6100. Another option is to use the high performance LT1787 current sense amplifier. The LT1787 plus an external sense resistor provides an easy, accurate, and compact solution for accurate, bidirectional current sensing. Current resolution greater than 1/10,000th can be achieved, even with low value, low insertion loss sense resistors. Specified for supplies from 2.5V to 60V, the LT1787 requires just 60µA max supply current.

Applications

Low Power, Current Monitor with 16-Bits of Resolution

The speed and accuracy of the LTC6101 makes it ideal for direct interface to an ADC, such as Linear Technology's 16-bit, Delta Sigma, LTC2433. Access to the input and output resistors allows the user to configure the optimal impedance while maintaining the desired gain. Using tiny surface mount components and two external resistors, this solution is efficient for space, as well as power. Typical current consumption for this circuit is under 500µA.

Why Two Resistors Are Better than One

The LTC6101 is a unique current sense amplifier. Unlike the competition, Linear Technology's design team chose to give the user control over R_{IN} and R_{OUT}, providing greater flexibility and performance. Consider the following advantages:

- **Using 0.1% resistors for R_{IN} and R_{OUT}, the user can achieve gain better than 0.2%**
- **By selection of R_{IN}, the user can trade off response time and power loss in R_{SENSE}**
- **The user has the flexibility to set both gain and output impedance for optimum output drive**
- **Optimal power consumption can be achieved by selecting a large R_{IN} to limit output current**
- **DC accuracy can be outstanding by selection of input resistors to cancel bias current error**

Details of these benefits can be found in the applications section of the LTC6101 datasheet, available at www.linear.com

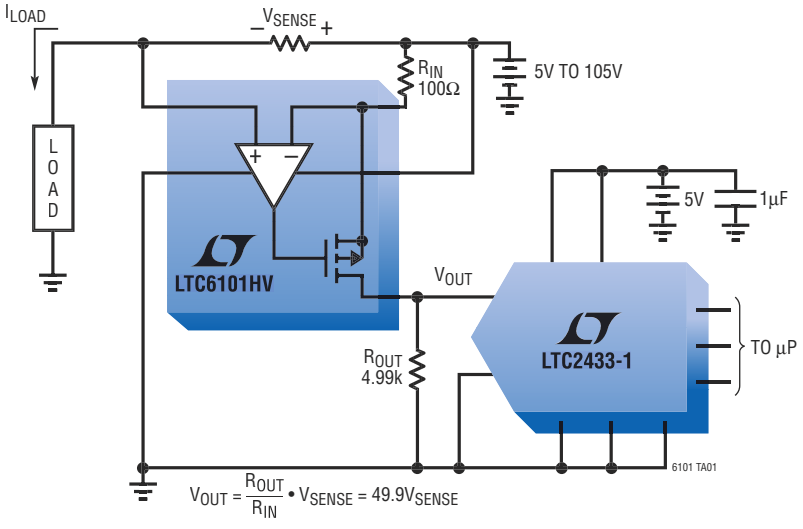


Figure 2. The LTC6101HV Easily Interfaces to an ADC

High Side Current Sensing

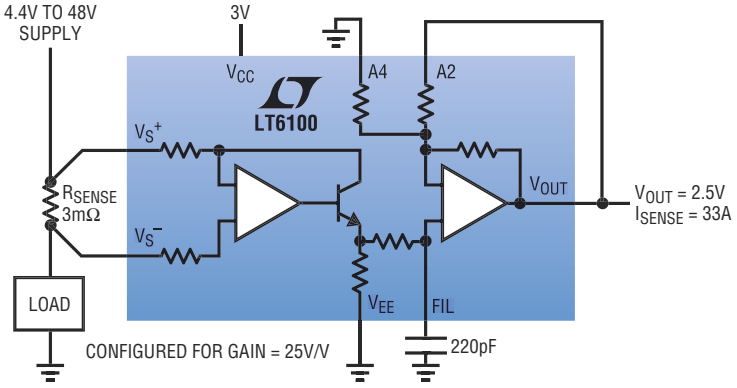


Figure 3. Gain is Selected by Pin-Strapping, No External Components Required

Get the Scoop on Current Sense

Visit www.linear.com for the I_{SENSE} Solutions Guide – an extensive collection of current sense circuits and discussion condensed from years of Linear Technology's experience. Among the topics discussed:

- **High Side and Low Side Current Sensing**
- **Unidirectional and Bidirectional Current Sensing**
- **High Current and Low Current Sensing**
- **Designing and Using PCB Current Sense Resistors**

0 to 33 Amp, High Side Current Monitor with 12kHz Frequency Rolloff

One of the simplest, most practical applications of the LT6100 is for use as a large dynamic range current monitor. Since it has only 300µV of offset voltage, using a 3mΩ shunt provides 100mA resolution with a full-scale range of 33A. In this circuit, the device is operated from a single 3V supply. When powered down, the LT6100 input is essentially "disconnected" from the system since it typically draws 1nA of input current. Connecting a 220pF capacitor at the filter input pin, FIL, provides a 12kHz differential noise rolloff, and configuring the internal resistors via pins A4 and A2 selects a gain of 25V/V.

Charge/Discharge Current Monitor on a Single Supply

By providing direct access to the output resistor of the LT1787, the output of this bidirectional part can be biased to a desired halfway point. In Figure 4, the output is biased for single supply operation by using an external voltage reference. The output signal can swing above and below the bias voltage to indicate positive or negative current through the sense resistor. In this example, the circuit can operate with a supply voltage as low as 3.1V.

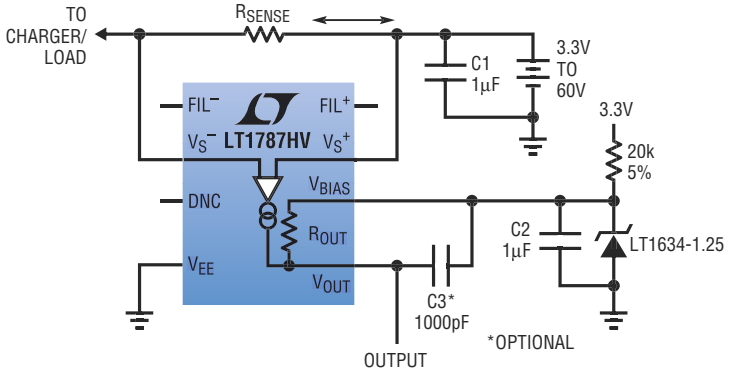


Figure 4. Biasing Allows the Output to Indicate Direction when Operating from a Single Supply

BY JIM WILLIAMS • LINEAR TECHNOLOGY CORP

Minimizing switching-regulator residue in linear-regulator outputs

BANISHING THOSE ACCURSED SPIKES TAKES ATTENTION TO DETAIL AND UNDERSTANDING THE SUBTLETIES.

Designers frequently use linear regulators to postregulate switching-regulator outputs. The benefits of this approach include improved stability, accuracy, and transient response, along with lower output impedance. Ideally, markedly reduced switching-regulator-generated ripple and spikes would accompany these performance gains. In practice, all linear regulators encounter some difficulty with ripple and spikes, particularly as frequency rises. The regulator's small input to output differential voltages magnify these effects; this situation is unfortunate, because such small differentials are desirable for maintaining efficiency.

Input-filter capacitors smooth the ripple and spikes before they reach the regulator (**Figure 1**). The output capacitor maintains low output impedance at higher frequencies, improves load transient response, and supplies frequency compensation for some regulators. Ancillary purposes include minimizing both noise and the appearance of residual-input-derived artifacts at the regulator's output. These artifacts are of concern because these high-frequency components, even though of small amplitude, can cause problems in noise-sensitive video, communication, and other types of circuitry. Designers expend large numbers of capacitors and aspirin in attempts to eliminate these undesired signals and their resultant effects. Although these signals are stubborn and sometimes seemingly immune to any treatment, understanding their origin and nature is the key to containing them.

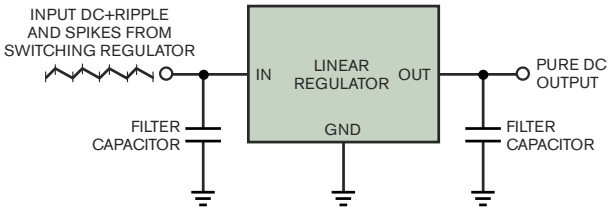


Figure 1 A conceptual linear regulator and its filter capacitors theoretically reject switching-regulator ripple and spikes.

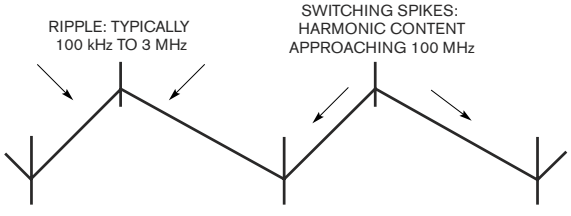


Figure 2 A switching-regulator output contains relatively low-frequency ripple and high-frequency "spikes," derived from regulators' pulsed-energy delivery and fast transition times.

SWITCHING-REGULATOR AC-OUTPUT CONTENT

Figure 2 details a switching regulator's dynamic ac-output content. It comprises relatively low-frequency ripple at the switching regulator's clock frequency—typically, 100 kHz to 3 MHz—and high-frequency content "spikes" associated with power-switch transition times. The switching regulator's pulsed

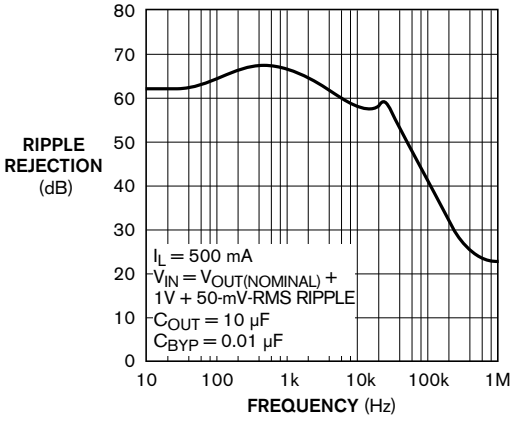


Figure 3 Ripple-rejection characteristics for an LT1763 low-dropout linear regulator show 40-dB attenuation at 100 kHz, rolling off toward 1 MHz. Switching-spike harmonic content approaches 100 MHz and passes directly from input to output.

energy delivery creates the ripple. Filter capacitors smooth—but do not eliminate—the ac content. The spikes, which often have harmonic content approaching 100 MHz, result from high-energy, rapidly switching power elements within the switching regulator. Slowing the regulator's repetition rate and transition times can greatly reduce ripple and spike amplitude, but the size of the magnetic elements increases, and their efficiency falls. Circuitry employing this approach has significantly reduced harmonic content but sacrificed the magnetics' size and efficiency (**Reference 1**). The same rapid clocking and switching that allows the use of small, highly efficient passives results in the presentation of high-frequency ripple and spikes to the linear regulator.

The regulator is better at rejecting the ripple than the wideband spikes. In a typical example, the rejection performance for an LT1763 low-dropout linear regulator, 40 dB of attenuation at 100 kHz rolls off to about 25 dB at 1 MHz (**Figure 3**). The more wideband spikes pass directly through the regulator. The output-filter capacitor, which absorbs the spikes, also has high-frequency performance limitations. The imperfect response of the regulator and filter capacitors, due to high-frequency parasitics, reveals **Figure 1** to be too simplistic. Including parasitic terms and some new components shows the regulation path with emphasis on high-frequency parasitic terms (**Figure 4**). It is important to identify these terms because they allow ripple and spikes to propagate into the nominally regulated output.

Additionally, understanding the parasitic elements permits a measurement strategy, facilitating reduction of high-frequency output content. The regulator includes high-frequency parasitic paths, primarily capacitive, across its pass transistor and into its

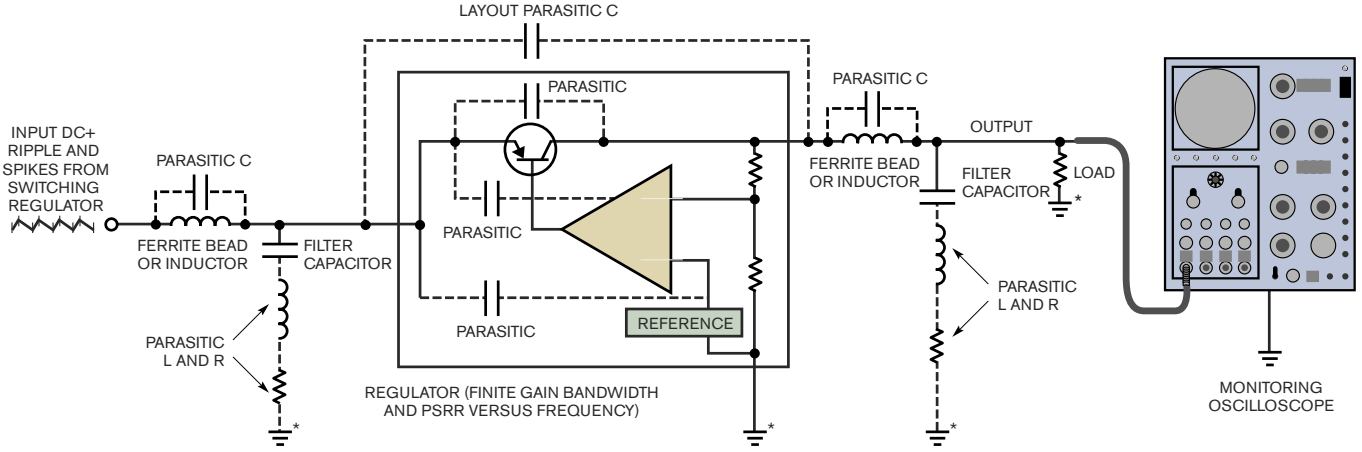


Figure 4 A conceptual linear regulator shows high-frequency-rejection parasitics. The finite-gain-bandwidth product and power-supply-rejection-ratio versus frequency limit the regulator's high-frequency rejection. Passive components attenuate ripple and spikes, but parasitics degrade effectiveness. The layout capacitance and ground-potential differences add errors and complicate measurement.

THE TRUTH ABOUT FERRITE BEADS

A ferrite bead enclosing a conductor provides the highly desirable property of increasing impedance as frequency rises. This effect suits high-frequency noise filtering of conductors carrying dc and low-frequency signals. The bead is essentially lossless within a linear regulator's passband. At higher frequencies, the bead's ferrite material interacts with the conductor's magnetic field, creating the loss characteristic. Various ferrite materials and geometries result in different loss factors versus frequency and power level (Figure A).

Impedance rises from 0.01Ω at dc to 50Ω at 100 MHz. As dc current and, hence, constant magnetic-field bias rise, the ferrite becomes less effective in offering loss. Note that you can stack beads in series along a conductor, proportionally increasing their loss contribution. A variety of bead materials and physical configurations are available to suit requirements in standard and custom products.

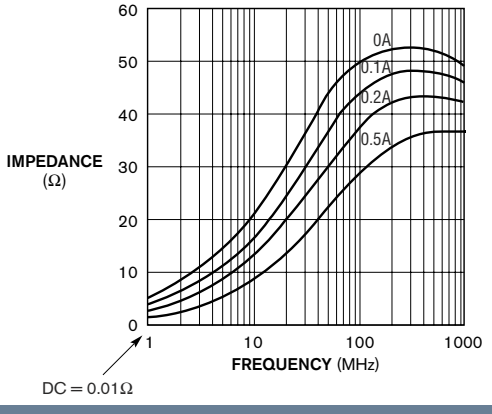


Figure A Impedance versus frequency at various dc-bias currents for a surface-mounted ferrite bead shows essentially zero impedance at dc and low frequency, rising above 50Ω depending on frequency and dc current (courtesy Fair-Rite).

Intersil Battery Charger ICs

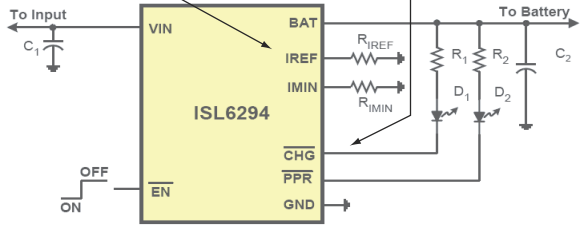
Intersil High Performance Analog

Have **YOU** Seen the World's Smallest Battery Charger IC?

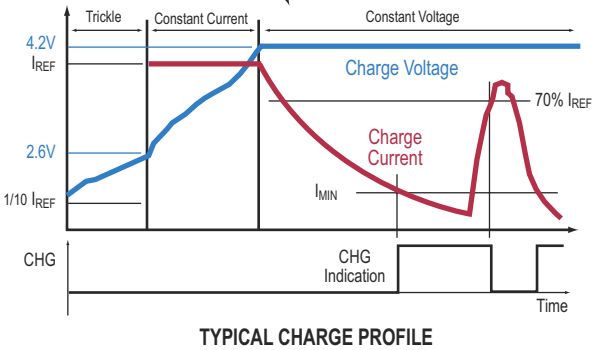
Not only is the 2mm x 3mm ISL6294 the industry's smallest, but this fully integrated, single-cell Li-Ion / Li-Polymer battery charger IC can handle input voltages up to 28V, eliminating the need for an over-voltage protection circuit.

The constant current I_{REF} is set with the external resistor R_{IREF}. The constant voltage is fixed at 4.2V.

End-of-charge (EOC) current indicated through the CHG pin (which can be interfaced to a micro processor), but the charger continues to output the 4.2V.



If the battery voltage is below 2.6V the ISL6294 charges the battery with a trickle current of one-tenth of I_{REF}. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates to fully charge battery without the risk of over charge.



TYPICAL CHARGE PROFILE

Key Features:

- 2mm x 3mm 8 Ld DFN package
- 28V maximum input voltage
- Programmable end-of-charge current with status interfaced to a micro device through CHG pin
- Thermaguard™ charge current thermal foldback for thermal protection
- No external blocking diode required
- Integrated pass element and current sensor
- 1% voltage accuracy
- Trickle charge for fully discharged batteries
- Less than 1µA leakage current off the battery when no input power attached or charger disabled
- Input over-voltage protection
- End-of-charge indication with large hysteresis to prevent unwanted re-charge

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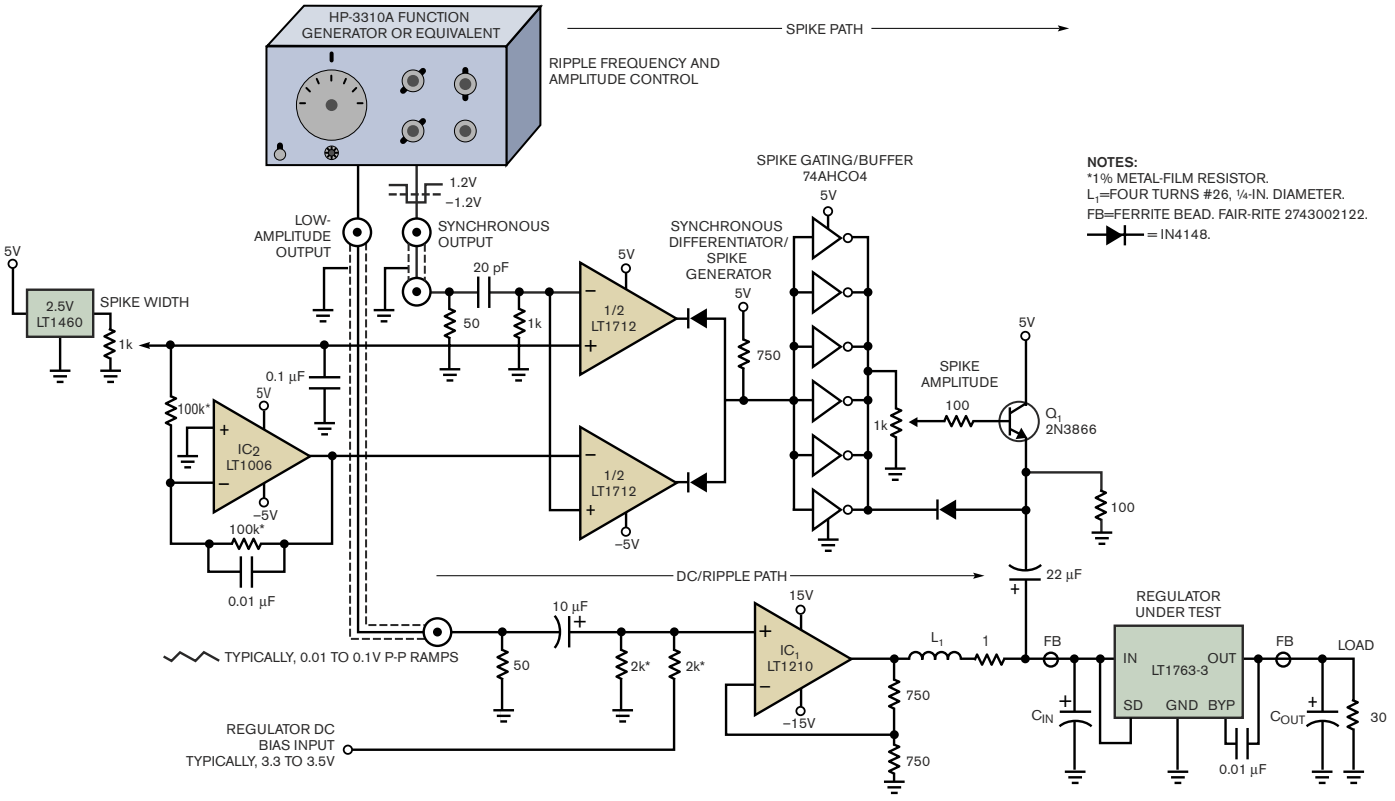


Figure 5 This circuit simulates switching-regulator output. You can independently set ripple amplitude, dc, frequency, and spike duration and height. A split-path scheme sums wideband spikes with dc and ripple, presenting the linear regulator with simulated switching-regulator output. A function generator sources waveforms to both paths.

USING INDUCTORS AS HIGH-FREQUENCY FILTERS

You can sometimes use inductors instead of beads for high-frequency filtering. Typically, values of 2 to 10 µH are appropriate. Advantages include wide availability and better effectiveness at frequencies of less than 100 kHz. Figure A shows that the disadvantages are increased dc resistance in the regulator path due to copper losses, addition of parasitic shunt capacitance, and potential susceptibility to stray switching-regulator radiation. The copper loss appears at dc, reducing efficiency, and parasitic shunt capacitance allows unwanted high-frequency feedthrough. The position and orientation of the inductors on the pc board may allow stray magnetic fields to impinge its winding, effectively turning the winding into a secondary transformer. The resulting observed spike- and ripple-related artifacts masquerade as conducted components, degrading performance.

Figure B shows a form of inductance-based filter constructed from a pc-board trace. Such extended-length traces, formed in spiral or serpentine patterns, look inductive at high frequencies. They can be surprisingly effective in some circumstances, although they introduce less loss per unit area than ferrite beads.

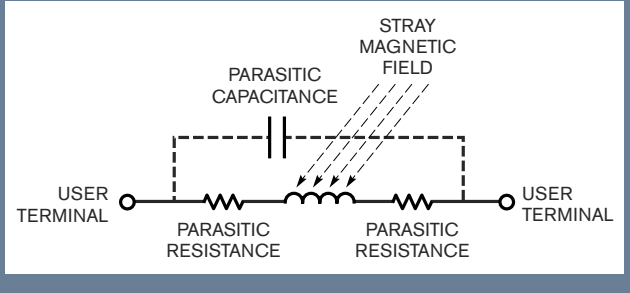


Figure A Some parasitic terms of an inductor show that parasitic resistance decreases voltage, degrading efficiency, and unwanted capacitance permits high-frequency feedthrough. The stray magnetic field induces erroneous inductor current.

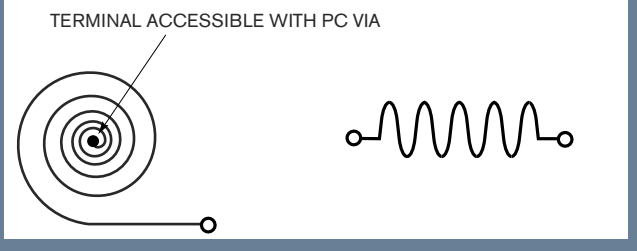
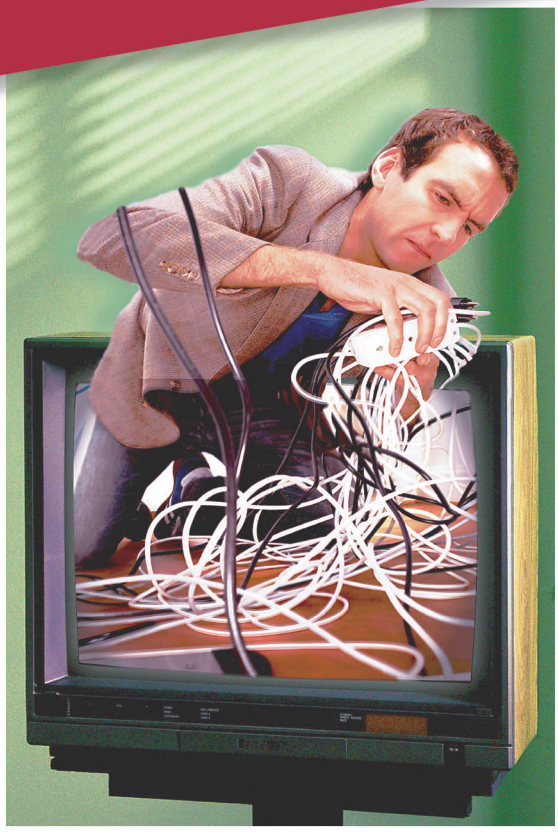


Figure B Spiral and serpentine pc-board patterns sometimes act as high-frequency filters, although they are less effective than ferrite beads.

Intersil Video Products

High Performance Analog

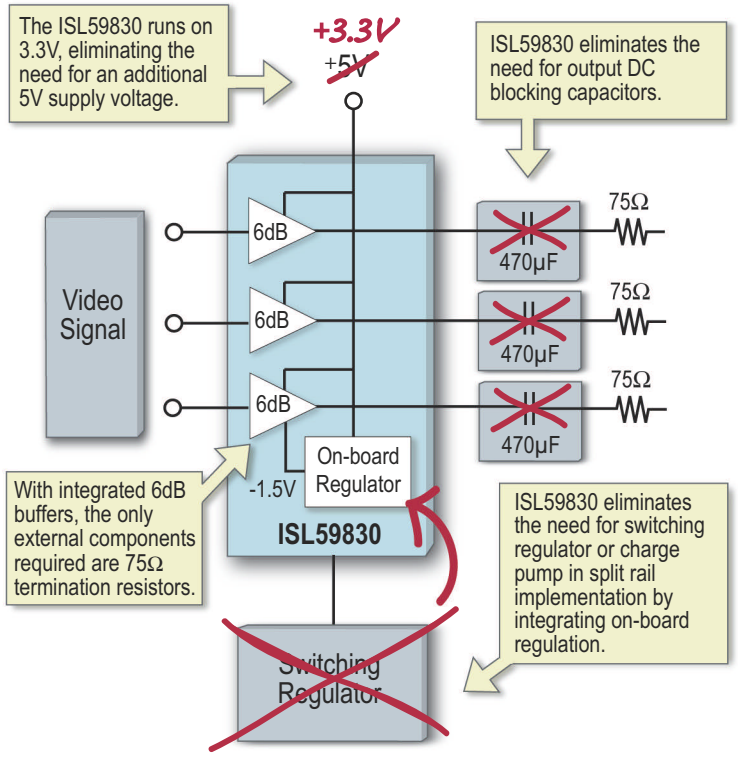
Why Tangle Up Your Video Design with an Extra Power Supply?



Finally...a true single-supply Video Buffer. Intersil's new ISL59830 not only operates on just +3.3V, but we've integrated the required negative voltage, eliminating the need for output DC blocking capacitors and external voltage regulation.

The ISL59830 triple Video Buffer delivers DC-accurate coupling of video onto a 75Ω double-terminated line, and 300MHz of -3dB bandwidth performance. Now that's smart design.

ISL59830 Functional Block Diagram



Key Features:

- Triple single-supply buffer
- Operates from single +3.3V supply
- Eliminates need for DC blocking capacitors
- Fixed gain of 2 output buffer
- Output 3-statable
- Enable/disable functions
- 50MHz 0.1dB bandwidth
- 300MHz -3dB bandwidth

Datasheet, free samples, and more information available at **www.intersil.com/edn**

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reference and regulation amplifier. These terms combine with finite regulator gain bandwidth to limit high-frequency rejection. The input- and output-filter capacitors include parasitic inductance and resistance, degrading their effectiveness as frequency rises. Stray layout capacitance provides additional unwanted feedthrough paths. Ground-path resistance and inductance promote ground-potential differences, which add error and also complicate measurement.

Some new components, not normally associated with linear regulators, also appear. These additions include ferrite beads or inductors in the regulator input and output lines. These components have their own high-frequency parasitic paths but can considerably improve overall regulator high-frequency rejection (see **sidebar** "The truth about ferrite beads").

BUILD A RIPPLE/SPIKE SIMULATOR

Understanding the problem requires observing regulator response to ripple and spikes under a variety of conditions. You should independently vary ripple and spike parameters, including their frequency, harmonic content, amplitude, duration, and dc level. This capability is versatile, permitting real-time optimization and sensitivity analysis to various circuit variations.

PROBING TECHNIQUE FOR SUBMILLIVOLT-WIDEBAND-SIGNAL INTEGRITY

Obtaining reliable, wideband, submillivolt measurements requires attention to critical issues before measuring anything. It is essential that you design the pc-board layout for low noise. Consider current flow and interactions in power distribution, ground lines, and ground planes. Examine the effects of component choice and placement. Plan radiation management and disposition of load-return currents. The circuit must be sound, the board layout must be proper, and the circuit must use the appropriate components before you can begin meaningful measurements.

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurately extracting information. Low-level, wideband measurements demand care in routing signals to test instrumentation. Issues to consider include ground loops between pieces of test equipment, including the power supply connected to the breadboard, and noise pickup due to excessive test-lead or trace length.

Minimize the number of connections to the pc board and keep leads short. Route wideband signals to or from the breadboard in a coaxial environment with attention to where the coaxial shields tie into the ground system. A strictly maintained coaxial environment is critical for reliable measurements.

Figure A shows a believable presentation of a typical switching-regulator spike measured within a continuous coaxial signal path. The spike's main body is reasonably well-defined, and disturbances after it are contained. Figure B depicts the same event with a 3-in. ground lead connecting the coaxial shield to the pc-board ground plane. Pronounced signal distortion and ringing occur. The photographs were taken at 0.01V/division sensitivity. More sensitive measurement requires proportionately more care.

Figure C details the use of a wideband, 40-dB gain preamplifier permitting a 200-μV/division measurement in Figure 12 of the main text (pg 90). Note the purely coaxial path, including the ac-coupling capacitor, from the regulator, through the preamplifier, and to the oscilloscope. The coaxial-coupling capacitor's shield directly connects to the regulator board's ground plane with the capacitor's center conductor going to the regulator output. There are no noncoaxial-measurement connections. Figure D, repeating Figure 12, shows a cleanly detailed rendition of the 900-mV output spikes. In Figure E, 2 in. of ground lead is present at the measurement site, violating the coaxial regime. The result is corruption of the waveform presentation. As a final test to verify measurement integrity, it is useful to repeat Figure D's measurement with the signal-

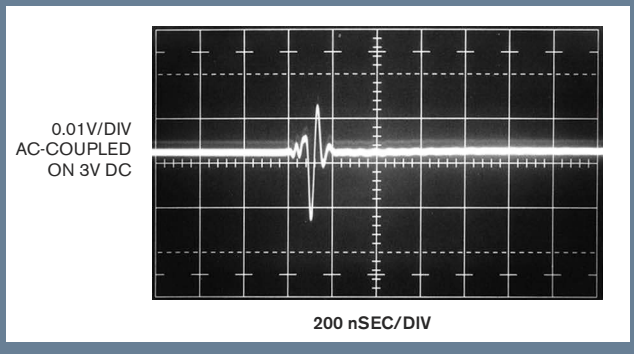


Figure A Spike measured within a continuous coaxial-signal path displays moderate disturbance and ringing after the main event.

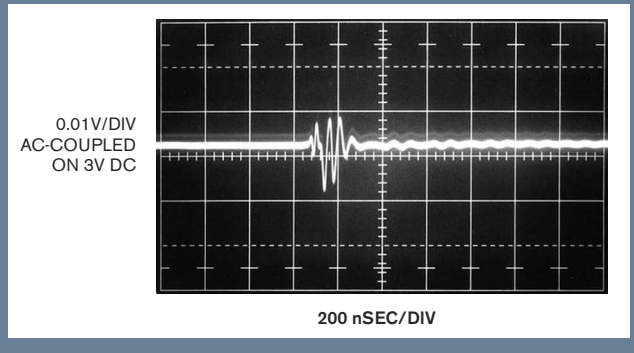


Figure B Introducing a 3-in., noncoaxial ground connection causes pronounced signal distortion and postevent ringing.

Although no substitute exists for observing linear-regulator performance under actual switching-regulator-driven conditions, a hardware simulator reduces the likelihood of surprises (**Figure 5**). It simulates a switching regulator's output with independently settable dc, ripple, and spike parameters.

The design combines a commercially available function generator with two parallel signal paths to form the circuit. It transmits dc and ripple on a relatively slow path and processes wideband spike information through a fast path. The two paths combine at the linear-regulator input. The function generator's settable ramp output (**Figure 6**, Trace A) feeds the dc/rip-

ALTHOUGH NO SUBSTITUTE EXISTS FOR OBSERVING LINEAR-REGULATOR PERFORMANCE UNDER ACTUAL SWITCHING-REGULATOR-DRIVEN CONDITIONS, A HARDWARE SIMULATOR REDUCES THE LIKELIHOOD OF SURPRISES.

path input–for example, the coaxial-coupling capacitor's center conductor–grounded near the measurement point, as in Figure 13 of the main text. Ideally, no signal should appear. Practically, some small residue, primarily due to common-mode effects, is permissible.

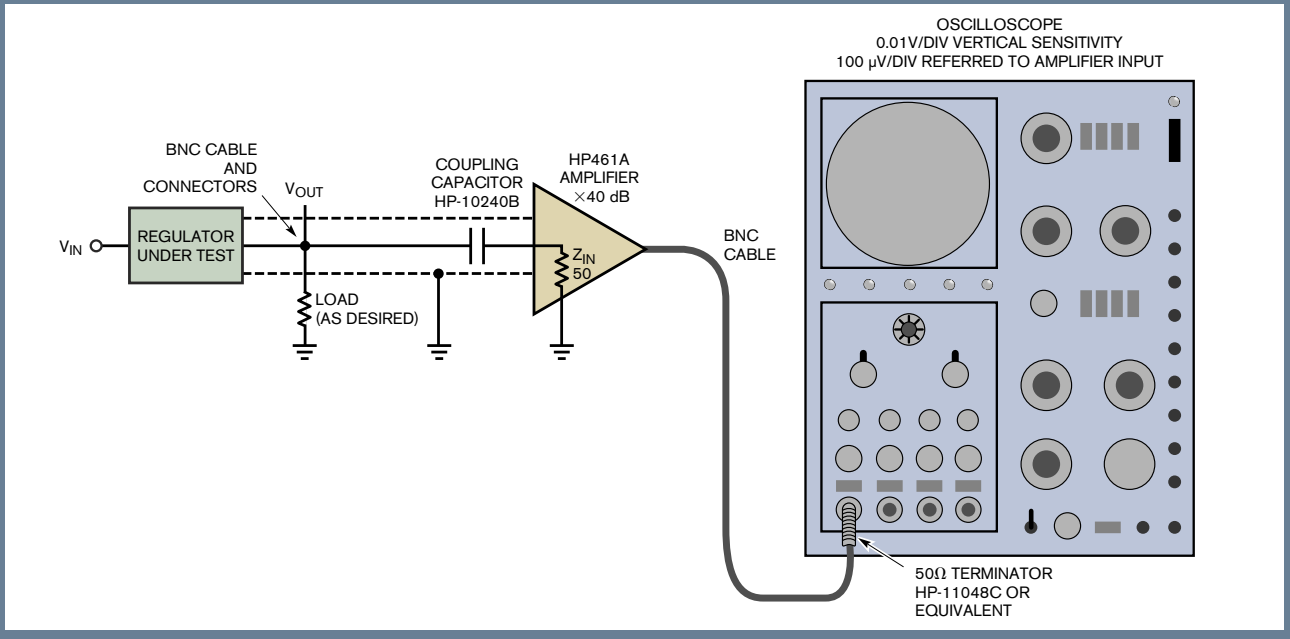


Figure C A wideband, low-noise preamplifier permits submillivolt-spike observation. The coaxial connections must remain to preserve measurement integrity.

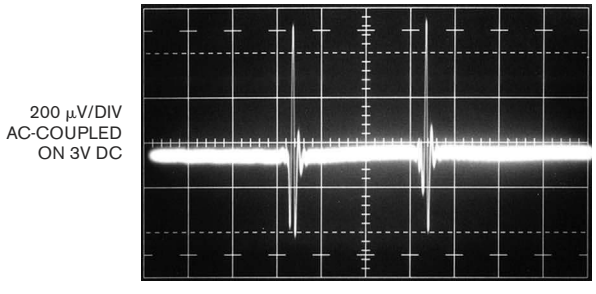


Figure D A low-noise preamplifier and strictly enforced coaxial signal path yield Figure 12's 900-mV p-p presentation. The trace's baseline thickening represents the preamplifier's noise floor.

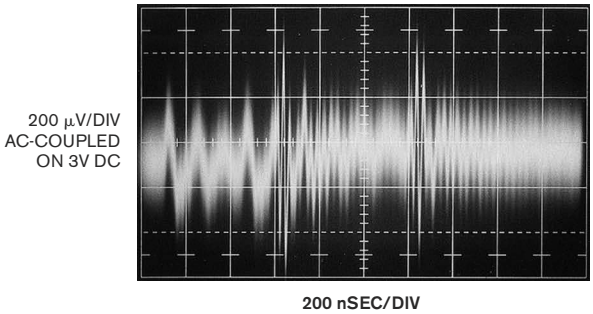
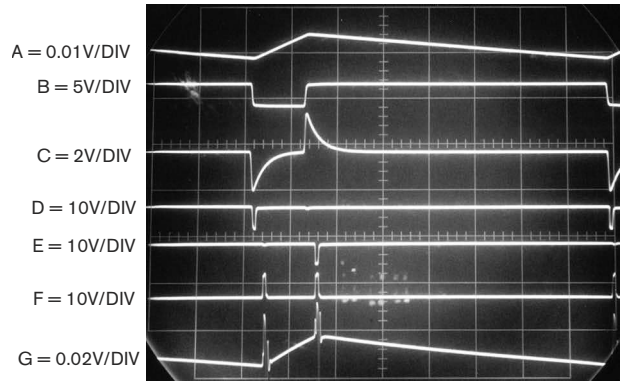


Figure E A 2-in. noncoaxial ground connection at the measurement site violates the coaxial regime, resulting in complete corruption of the waveform presentation.



NOTE: AC-COUPLED ON 3.3V DC.

Figure 6 A switching regulator outputs simulator waveforms, in which the function generator supplies ripple-path (Trace A) and spike-path (Trace B) information. C_1 and C_2 compare the differentiated spike information's bipolar excursion (Trace C), resulting in Traces D and E's synchronized spikes. Diode-gating inverters present Trace F to spike-amplitude control. G_1 sums spikes with dc-ripple path from power amplifier IC_1, forming linear-regulator input (Trace G). (Spike width is abnormally wide for photographic clarity.)

ple path, which is made up of power amplifier IC_1 and associated components. IC_1 receives the ramp input and dc-bias information and drives the regulator under test. L_1 and the 1Ω resistor allow IC_1 to drive the regulator at ripple frequencies without instability.

The function generator's pulsed synchronous output (Trace B) sources the wideband spike. Amplifier IC_2 differentiates the output's edges (Trace C) and feeds bipolar comparator IC_{3A} and

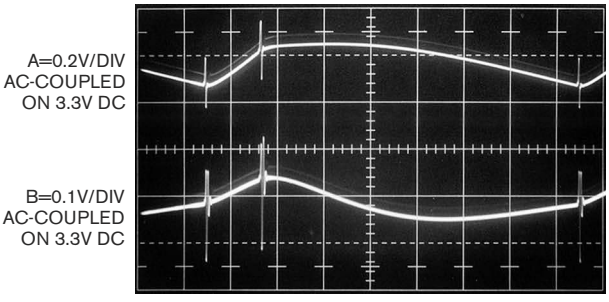


Figure 7 C_{IN} of 1 µF and C_{OUT} of 10 µF result in linear-regulator input (Trace A), output ripple (Trace B), and switching-spike content. Output spikes, driving 10 µF, have lower amplitude, but rise time remains fast.

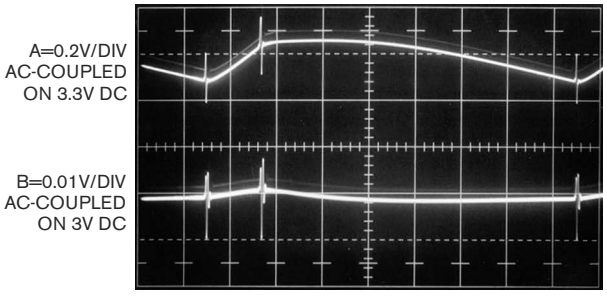


Figure 8 C_{IN} of 1 µF and C_{OUT} of 33 µF result in the same trace assignments as Figure 7. Output ripple decreases fivefold, but spikes remain. Spike rise time appears unchanged.

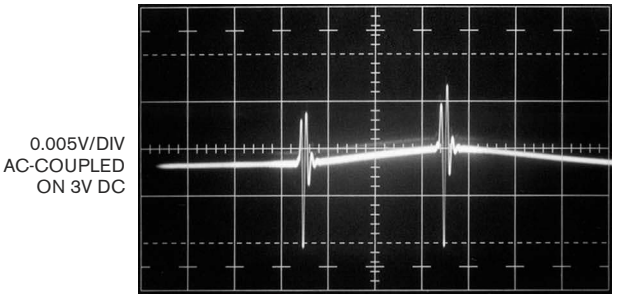


Figure 9 A time and amplitude expansion of Figure 8's output trace permits higher resolution study of spike characteristics. (The trace center-screen area is intensified for photographic clarity.)

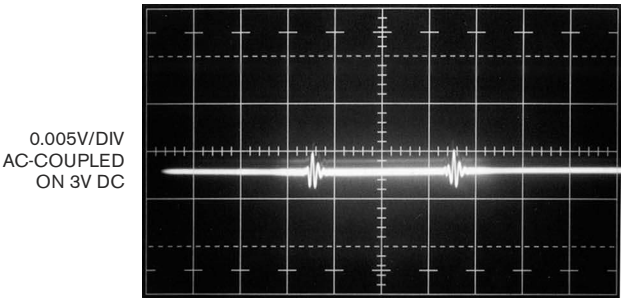


Figure 10 Adding a ferrite bead to the regulator input increases high-frequency losses, dramatically attenuating spikes. (The trace center-screen area is intensified for photographic clarity.)

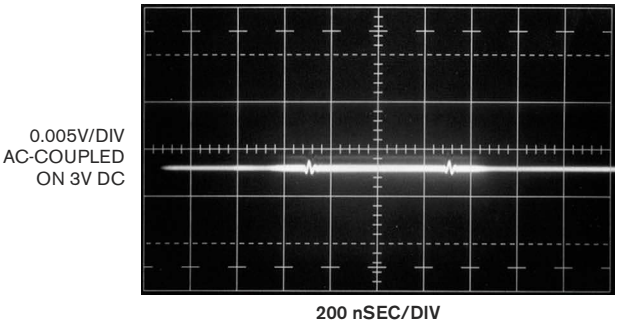


Figure 11 A ferrite bead in the regulator output further reduces spike amplitude. (The trace center-screen area is intensified for photographic clarity.)

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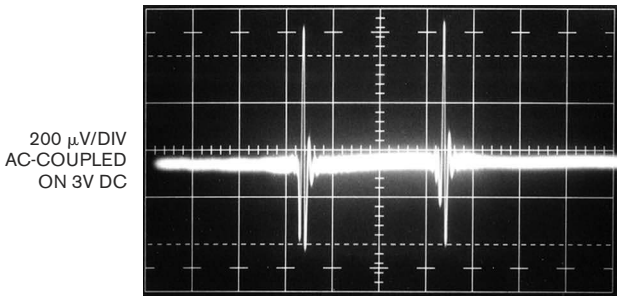

Figure 12 In this higher gain version of Figure 11, spike amplitude measures 900 μV—almost 20 times lower than without ferrite beads, whereas the instrumentation noise floor causes trace baseline thickening. (The trace center-screen area is intensified for photographic clarity.)

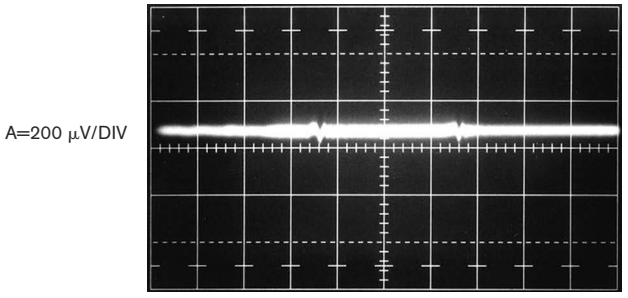

Figure 13 Grounding the oscilloscope input near the measurement point verifies that Figure 12's results are nearly free of common-mode corruption. (The trace center-screen area is intensified for photographic clarity.)

IC_{3B}. The comparator-output spikes (traces D and E) are synchronized to the ramp's inflection points. Complementary dc-threshold potentials applied to IC_{3A} and IC_{3B} with the 1-kΩ potentiometer and IC_2 control the spike width. Diode gating and the paralleled logic inverters present Trace F to the spike-amplitude control. Follower Q_1 sums the spikes with IC_1's dc/ripple path, forming the linear regulator's input (Trace G).

LINEAR-REGULATOR REJECTION EVALUATION

The circuit in **Figure 5** facilitates evaluation of linear-regulator high-frequency rejection. The waveform in **Figure 7** shows **Figure 5**'s LT1763 3V regulator response to a 3.3V-dc input with Trace A's ripple/spike contents, C_{IN}=1 μF, and C_{OUT}=10 μF. Regulator output (Trace B) shows ripple attenuated by a factor of approximately 20. Output spikes see somewhat less reduction, and their harmonic content remains high. The regulator offers no rejection at the spike's rise time. The capacitors must do the job. Unfortunately, inherent high-frequency loss terms prevent the capacitors from filtering the wideband spikes; Trace B's remaining spike shows no rise-time reduction. Increasing the capacitor value has no benefit at these rise times. **Figure 8**, with the same trace assignments as **Figure 7** but with a value of 33 μF for C_{OUT}, shows a fivefold ripple reduction but little spike-amplitude attenuation.

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Figure 9's time and amplitude expansion of **Figure 8**'s Trace B permits high-resolution study of spike characteristics, allowing the following evaluation and optimization. **Figure 10** shows dramatic results when a ferrite bead immediately precedes C_{IN}. Spike amplitude drops about fivefold. The bead presents loss at high frequency, severely limiting spike passage. The dc and low-frequency components pass unattenuated to the regulator. Placing a second ferrite bead at the regulator output before C_{OUT} produces **Figure 11**'s trace. The bead's high-frequency loss characteristic further reduces spike amplitude below 1 mV without introducing dc resistance into the regulator's output path. You can sometimes use inductors in place of beads, but make sure that you understand inductors' limitations (see **sidebar** "Using inductors as high-frequency filters").

Figure 12, which shows a higher gain version of **Figure 11**, measures 900-μV spike amplitude—almost 20 times lower than without the ferrite beads. Complete the measurement by verifying that common-mode components or ground loops do not corrupt the indicated results. You achieve this goal by grounding the oscilloscope input near the measurement point. Ideally, no signal should appear. **Figure 13** shows almost no signal, indicating that **Figure 12**'s display is realistic. Faithful wideband measurement at submillivolt levels requires special considerations (see **sidebar** "Probing technique for submillivolt-wideband-signal integrity"). The articles, application notes, and books in **references 2** through **9** are also helpful to serious designers. EDN

AUTHOR'S BIOGRAPHY

Long-time EDN *contributor Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), has more than 20 years' experience in analog-circuit and instrumentation design.*

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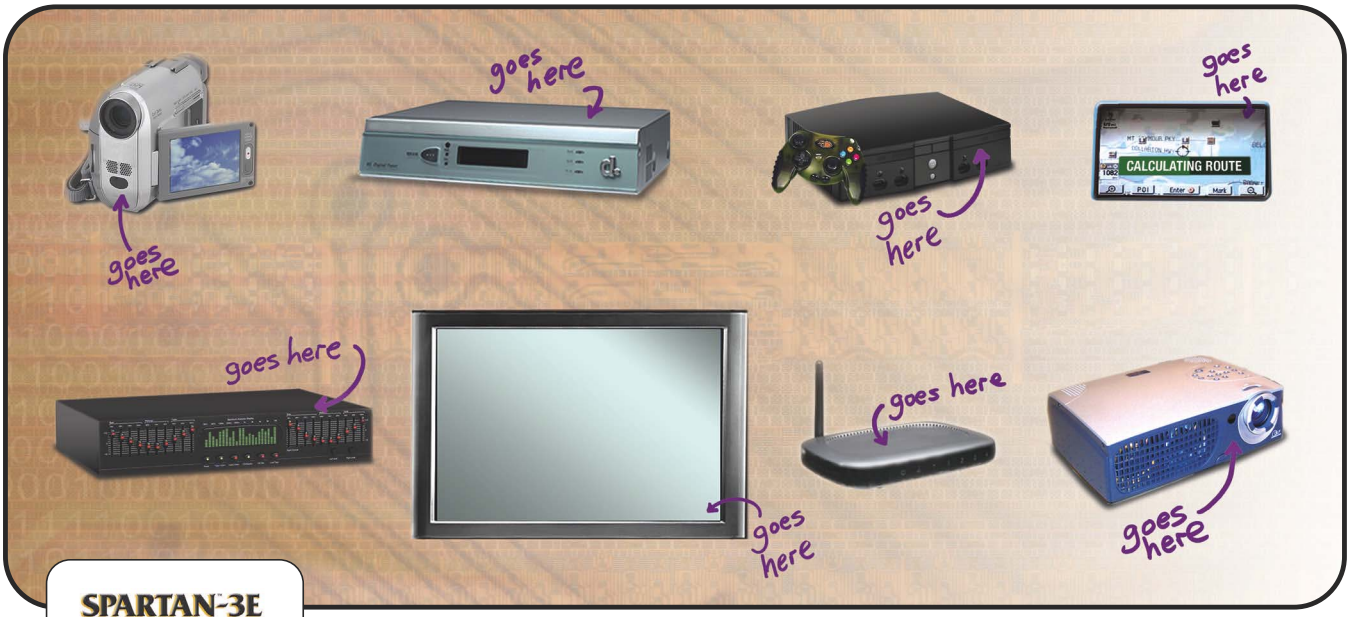

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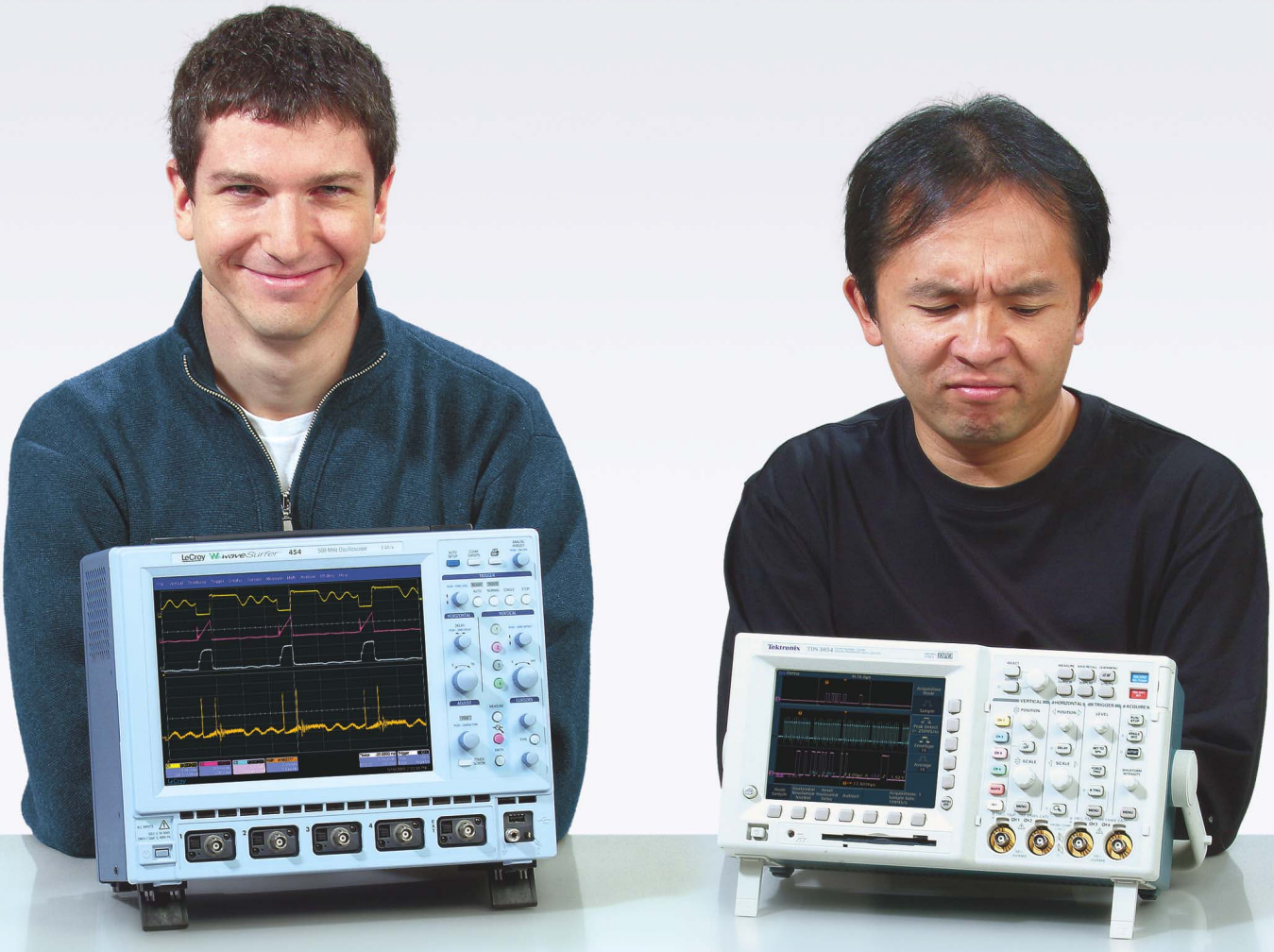

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Simplifying industrial backplanes

SYSTEM DESIGNERS TURN TO SERIAL-COMMUNICATIONS STRATEGIES TO BOOST RELIABILITY AND EXTEND SERVICE LIFE IN HOSTILE FACTORY OR INDUSTRIAL ENVIRONMENTS.

Designing automation controls for a factory floor is a daunting task. You must consider the environment—hot, dirty, corrosive, electrically noisy, and generally hostile to anything electronic (or human, for that matter). Most PLC (programmable-logic-controller) systems include a central controller and peripheral I/O modules. These modules can include ADCs, DACs for connecting to sensors and the real world, communications modules, digital inputs and outputs, relays, and more. All of these modules need to communicate with the central controller through a signal bus. Designers can bolster the reliability of a system by simply removing interconnections between devices. Several methods for this technique exist, but the simplest is to serialize the data and use fewer connections. The techniques involve several physical layers and topologies, as well as packet formats to make implementing these buses straightforward. Communication, whether it is with smoke signals or lasers, requires a physical medium in addition to some time to propagate from the origin to the destination. Many options are available, including wireless, cable, fiber optic, and acoustic. All of these physical media carry intelligence, but some are better than others for harsh environments.

In the wired category, the standards include TTL (transistor-to-transistor logic), ECL (emitter-coupled logic), RS232, RS422, RS485, LVDS (low-voltage differential signaling), and Ethernet, which find use in networks, backplanes, and buses. The older TTL standard uses a nearly 5V signal relative to ground; is slow; and is single-ended, which leaves it susceptible to ground noise. RS232 adds a bipolar voltage swing to help with noise immunity but lacks differential signaling's advantages in electrically noisy environments. RS422, RS485, and LVDS standards all use differential pairs of wires to remove common-mode noise across both wires at the receiver. LVDS uses current instead of voltage and greatly speeds the signaling by reducing signal swing. This approach removes many issues with wires, including cable capacitance.

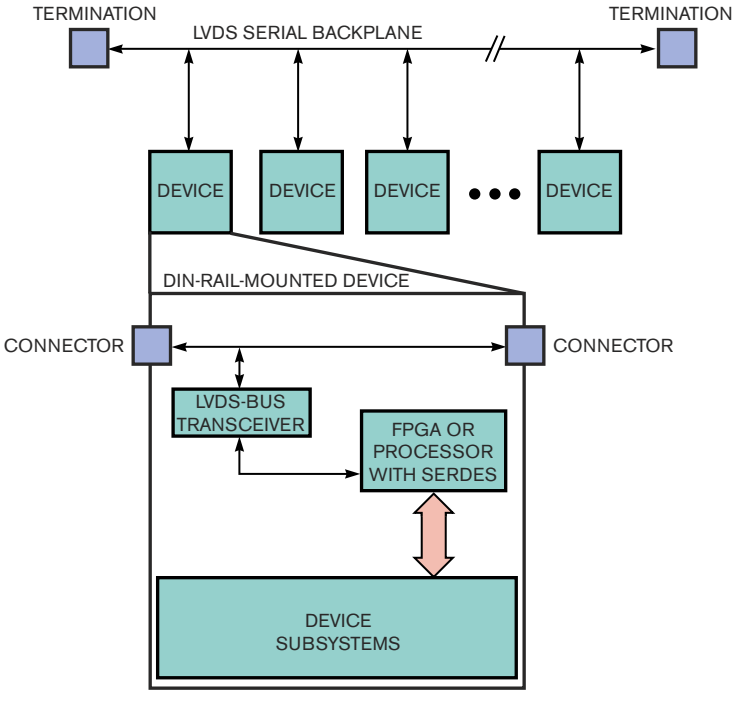

Figure 1 Many backplanes employ a multidrop serial bus to interconnect LVDS transceivers at each board.

In an electrically hostile environment, such as a steel mill, large electrical currents can be flowing inches away from a control system. These currents can induce noise onto conductors, especially long interconnects between devices. The standard technique for rejecting this noise is to use differential signaling. RS422 and RS485 are good options for long-haul interconnections but lack speed for local buses. LVDS is a better choice for local buses, such as those between devices mounted on DIN rails. In addition, designers are starting to use Ethernet as an interconnect in backplanes. Ethernet has several advantages. It is a standard; uses a well-defined MAC (media-access controller), which many processors employ; and has standard drivers for most operating systems. This article focuses on serialized-LVDS approaches as methods for maintaining good noise immunity plus providing 100- to 400-MHz speeds.

TOPOLOGIES

Which topology makes the most sense? Options include the multidrop bus, the redundant multidrop bus, the point-to-point bus, and the ever-

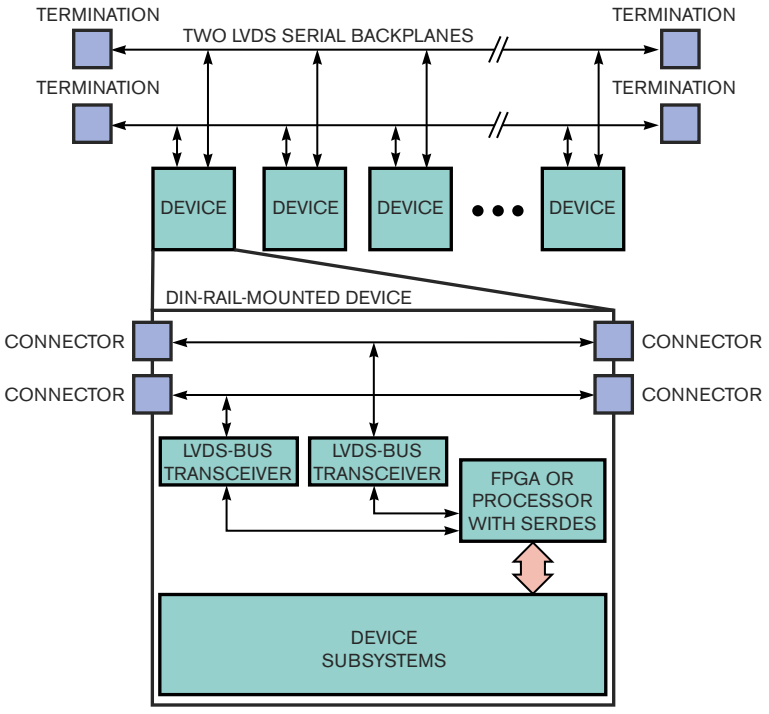

Figure 2 Dual multidrop buses prevent a single failure from disrupting operation and double the system bandwidth.

popular ring topology. The multidrop, or multipoint, bus is popular for many backplanes and is well-suited for both single- and multiple-processor systems. If you choose LVDS, you would use a double-terminated transmission line with LVDS transceivers at each board. The advantage of using individual transceivers is twofold. First, you can place the transceivers near the connector, limiting near-end reflections from the connection discontinuities. Second, these transceivers tend to be more robust than integrated drivers in FPGAs. They are also cheaper to replace in case of failure than a $100 FPGA. In this topology, a message would enable the driver on a board and send the serialized packet onto the backplane. All other devices would be listeners and receive the transmitted packet. Most shared-bus topologies need some form of traffic control. A simple method is to use a common access line involving additional wires to indicate to all devices that someone has requested the bus and no other device can talk. Alternatively, you can implement a master/slave organization to allow communication only when the master controller asks for it (**Figure 1**).

Multidrop buses are simpler to implement; however, the entire bus can fail if a single failure, such as a short, the loss of a terminator, or a hung bus driver, occurs. This failure can be catastrophic in an industrial environment; consider an oil refinery in which failure is not an option. A simple way to fix this problem is to use two buses. If one dies, the other keeps working. In addition to the redundancy, the system has twice the bandwidth in its native mode (normal operation). With two buses, the loss of one bus simply halves the available bandwidth, allowing the system to continue to function in a reduced mode. The downside to this option is increased cost and complexity (**Figure 2**).

Another method of preventing bus failures is to use a point-to-point topology, which Ethernet networks use. Each device has its own bus to communicate with the controller. If a single device or bus fails, all the other devices continue working without compromise. However, in a local backplane, the downside is the mechanical interconnection. For devices that plug into one another, such as DIN-rail mounting, pass-through con-

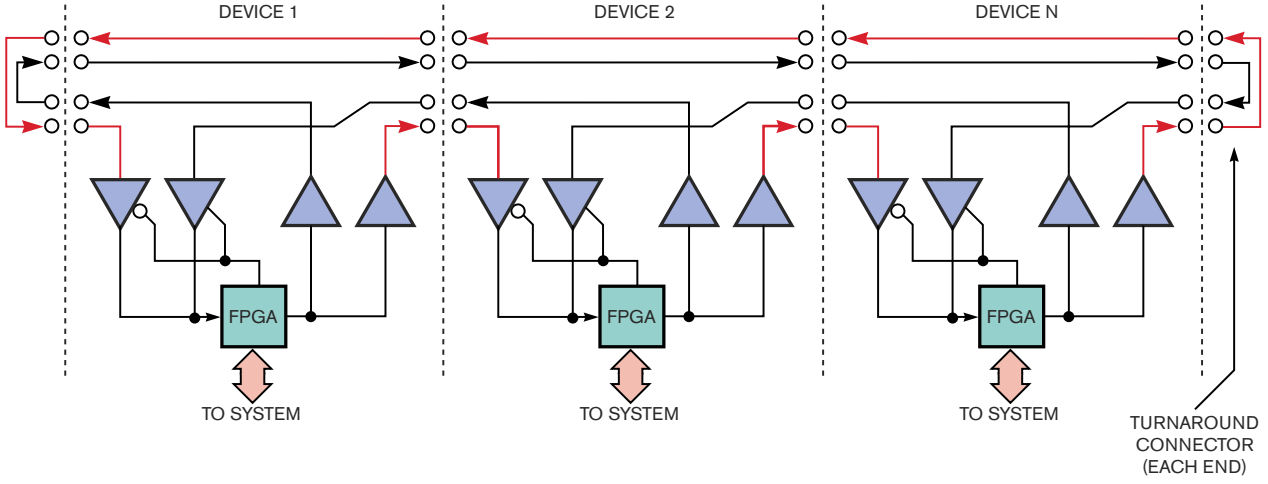

Figure 3 This three-device ring-topology example is self-healing and provides for automatic partitioning.

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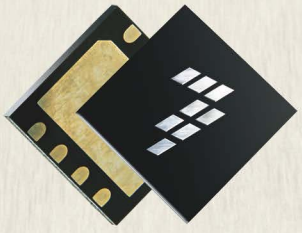

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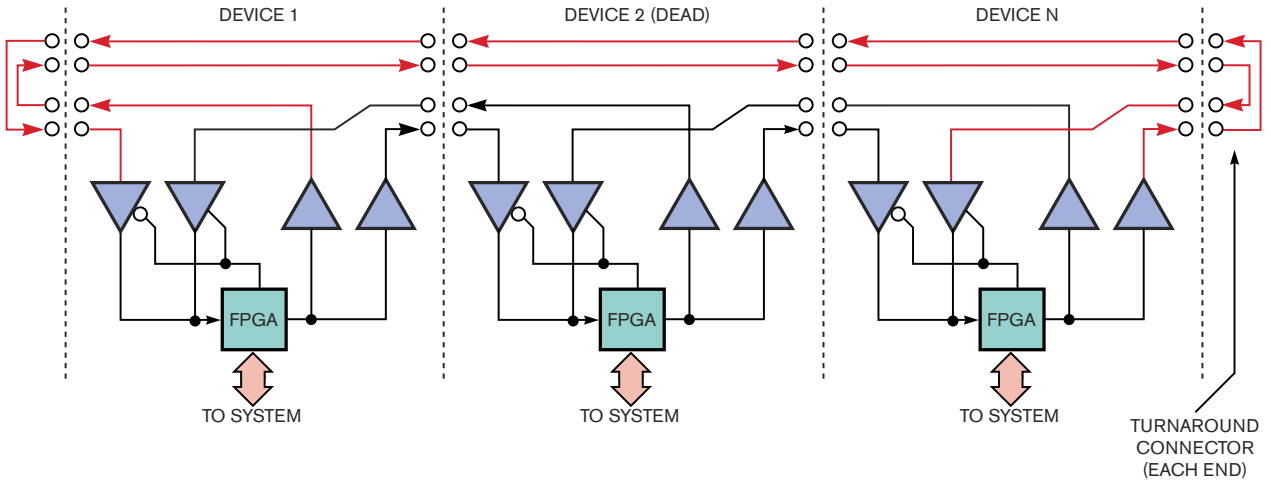


Figure 4 A ring topology using an FPGA-bus controller offers a simple method for implementing a TCP/IP-over-Ethernet backplane.

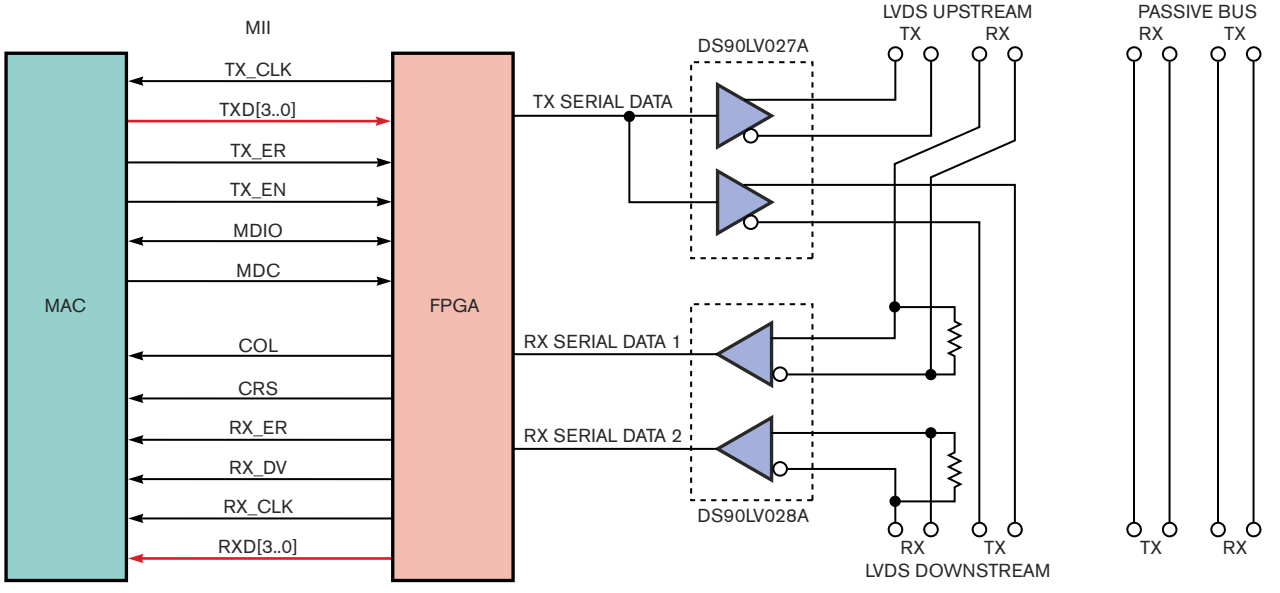


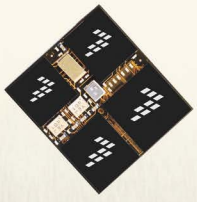
Figure 5 Ethernet provides a simple method for implementing an Internet-ready backplane.

nections would be necessary, thus increasing rather than minimizing the number of interconnections. The increased number of wires diminishes the advantages of the point-to-point topology for backplanes.

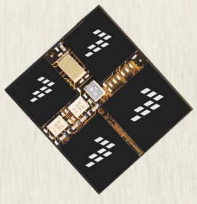
A ring topology, on the other hand, is self-healing and can automatically partition itself. Token-ring and similar networks use this method. In a backplane implementation, the system contains the ring. The topology also allows side-by-side plugging of modules on DIN rails (**Figure 3**). If any device or interconnection fails, the ring can turn back on itself, isolating the faulty device or broken connection (**Figure 4**). The physical implementation of the ring topology is similar in expense to that of a dual-multidrop-bus architecture with the exception of the interface. The ring uses only drivers and receivers, not transceivers. However, two additional passive buses are necessary to complete the ring. The driver is always enabled; however, because the device can select either of two receiver buses, an enable must select the desired bus. Alternatively, two digital inputs on an FPGA could select the bus. Sample components for this approach include the National Semiconductor DSLV-049, using digital selection of the receiver; the DS90LV027 and 28; or two DS90LV019 transceivers.

An interesting benefit of the ring topology is a pseudo-point-to-point connection. This approach eliminates the requirement for bus access because the packet traffic is unidirectional. The downside is that every module needs to handle every packet. Designers can somewhat automate this process in the control logic of the interface using a short buffer to implement a store-

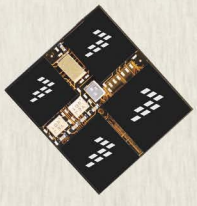
3G Solutions



It’s the freedom of an open platform.



It’s the freedom to miniaturize.



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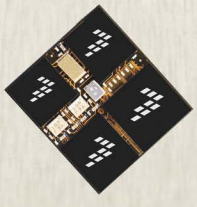
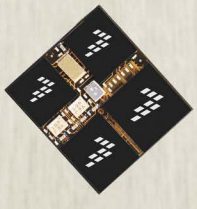


It’s the freedom to differentiate.



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and-forward methodology. The device need not necessarily store the entire packet but must store just the header for inspection.

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PROTOCOLS

Given a reliable hardware implementation, a method of accessing the physical media through a protocol is necessary. The protocols vary depending on the topology. In the multidrop topology, a device must signal to all the units before transmitting data to minimize or avoid collisions on the shared media. Collisions will occur, so a checksum must verify the integrity of the information in a packet of data. Randomization of retransmission times can help to reduce the collisions on the bus. Prioritizing devices by bus position or address can also help. By using a priority-access method, the units with the highest priority have the shortest wait time when sending packets. You can establish a fixed priority or use a round-robin approach in which the last device that transmitted has the lowest priority. As other devices send messages, the priority of the waiting device rises, and waiting time lowers. This method gives each device equal bus time to send messages. High-priority messages can have a fixed minimal delay time or no delay time for urgent messages, such as "emergency stop."

In a serializer/deserializer system, when the bus is not in use, idle messages continuously transmit to allow the recovery circuitry in the deserializer to synchronize on the data. In a shared-bus topology, the system cannot use idle messages to synchronize the receivers, so a preamble in the packet format is necessary. The preamble varies in length depending on how fast the receiver synchronization circuits lock to the incoming data. A faster lock time in the receiver means that the preamble will be shorter and the data throughput will be more efficient.

In a ring topology, it is advantageous to continuously transmit idle data to always lock the serializer/deserializer receivers. However, a method must exist for controlling when each device wishes to place information in the stream and not collide with another device. Ring topologies use token passing to provide a cue on when to transmit data. A token is a special header that identifies the current token master, as well as other data on the network. Data follows the token like freight cars following a locomotive. At each stop along the way, a device has the option of adding data following the token when the token is not in use.

In the simplest form of a ring, only one device can use the token at a time. This approach simplifies carrying packets in a continuous stream. So, as each device receives the token, it sets a bit in the token, signaling that it has taken the token for packet traffic, and all upstream devices, excluding the destination, simply pass it on. This method removes the store-and-forward requirement. The destination device simply removes

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the packet as it comes in and frees the token unless an outgoing packet needs it. The downside here is bus efficiency. If the token is in use, a device must wait for it to be free before sending data.

Various methods exist for providing priority to a token-based system. A simple one is to implement a round-robin method of token counting. If a system has three bits of priority (seven levels), once a device uses a token, the priority would drop to the seventh and lowest level. As the system passes the free token around, every time the token passes a device, the priority count increases by one until it reaches level zero, or "transmit ready." If the device has a packet pending, and a free token passes, it can now grab the token for itself. If an emergency occurs, the system can ignore the priority level and use the next free token.

Token protocols can be complex. For example, what happens if a device dies while it has the token? Also, when a user powers up the system, which device instantiates the token? Despite these issues, token passing works and can provide a self-healing system for highly reliable backplanes.

SAMPLE DESIGN

Many microcontrollers today, such as the Zilog EZ80 Acclaim and the Freescale MCF523x, have a built-in Ethernet MAC, which connects to a PHY (physical)-layer chip using an MII (media-independent interface). The MII has a 4-bit-data, nibble-mode interface along with a simple serial bus to configure the PHY. You can build a custom bus controller in an FPGA that has an MII to emulate an Ethernet PHY. The FPGA-based controller handles the bus access or token management, serialization and deserialization, ring management, healing, and clock generation and recovery.

This design can enable a system to transport Ethernet packets as if the backbone were Ethernet. Additionally, TCP/IP over Ethernet is well-defined and provides a simple method for implementing an Internet-ready backplane (**Figure 5**). The FPGA emulates the functions of the Ethernet PHY and allows the MAC inside the microcontroller to function as if connected to a normal Ethernet network.

Using LVDS eliminates many of the problems of noise in industrial environments. Also, speeds can increase through the use of current-mode drivers and lower voltage swings. In addition, by serializing data and reducing the number of interconnects between modular devices, LVDS increases reliability by avoiding connector failure. The sample design requires only eight upstream and eight downstream connections, providing a 100-Mbps, packet-based, Ethernet, self-healing ring topology. EDN

AUTHOR'S BIOGRAPHY

Richard Zarr is the worldwide program manager for technology-partnership marketing at National Semiconductor (Santa Clara, CA). He has a bachelor's degree in electrical engineering from the University of South Florida (Tampa, FL). His career involved designing computers and communication equipment before he entered applications engineering in 1984. His current focus is developing technology partnerships between National Semiconductor and other corporations requiring high-performance analog technologies.

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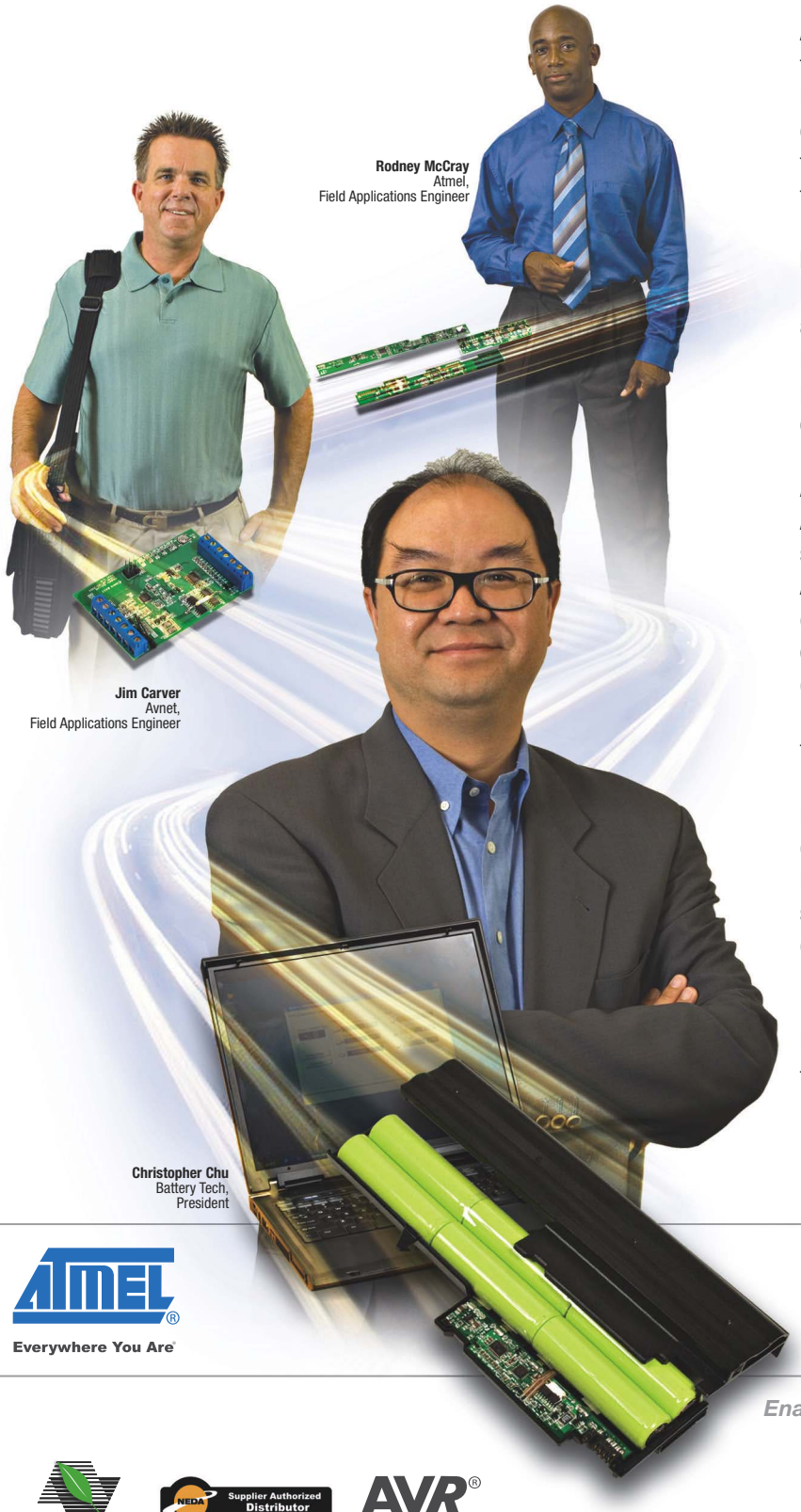
For additional application solutions and to download the BTI case study, visit: www.em.avnet.com/atmel/satb



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BY CHET DOUGLAS AND BOJI TONY KANNANTHANAM • INTEL

Common-driver-library architecture supports, maintains products

USING A CDL-BASED ARCHITECTURE FOR DEVICE DRIVERS CAN SIGNIFICANTLY REDUCE THE TIME TO DEVELOP, MAINTAIN, VALIDATE, AND SUPPORT DEVICE DRIVERS FOR MULTIPLE PLATFORMS.

With the plethora of operating systems available, a common problem for an independent hardware vendor is how to develop, maintain, and support device drivers for products. Although using a CDL (common driver library) can apply to any OS, the storage-device-driver example in this article focuses on Linux and Microsoft Windows. To make a CDL design work, a device-driver designer must understand and compartmentalize the typical driver functions into OS-specific and OS-agnostic functions. In this schema, the designer partitions a device driver into two logical sections based on its dependence on the operating system. Most of the driver code resides in the CDL, which essentially contains the hardware-specific function of the firmware interface, and it is OS-agnostic. The other section of the device-driver code acts as the glue that ties the common portion to an OS. The OS-dependent portion further divides into the CDHI (common-driver-host-interface) and CDHS (common-driver-host-services) layers (**Figure 1**).

The CDHI layer bolts the driver into the kernel. A typical device driver uses a kernel-specific API (application-programming interface) that all driver writers must use to register the driver with one or more kernel subsystems, such as the PCI, I/O, storage, or network. The API also provides the mechanism for the driver to learn of events such as an interrupt, I/O request, or I/O abort. The CDHI layer encapsulates this function and translates OS-specific routines to CDL routines; it comprises a well-defined API and mechanism to interface with the OS kernel.

The CDHS layer uses the services that the OS provides. A device driver also uses services the OS provides to manage the hardware it controls. These services include accessing system registers; communicating over I/O systems, such as PCI and PCI Express; and how to request, manipulate, and dispose of DMA memory, kernel virtual memory, and synchronization mechanisms, such as locks, "spin locks," and semaphores. (A spin lock is a busy-wait method of ensuring mutual exclusion for a resource. Tasks waiting on a spin lock sit in a busy loop until the spin lock becomes available.) A driver may also use special OS features such as "sysfs" support under Linux and event tracing under Windows. These functions, which the kernel architecture and API to a large extent dictate, tie closely to the capabilities of the OS. These OS-specific functions, on which the driver depends for its efficient operation, group together in the CDHS portion. The CDL uses the services that the CDHS interface provides and ensures that the CDL code remains OS-independent.

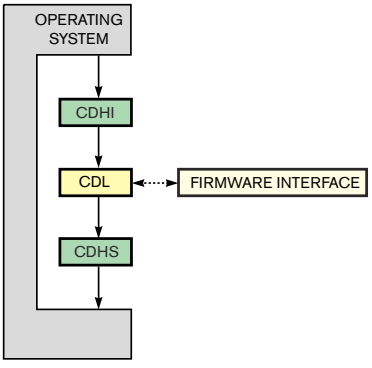

Figure 1 The OS-dependent portion of a CDL divides into the CDHI (common-driver-host-interface) and CDHS (common-driver-host-services) layers.

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The CDL resides between the CDHI and the CDHS layers. The CDL, the device-specific portion of the driver, is the core component that is aware of the hardware it controls. The intelligence of the device driver resides in the CDL. Typically, a driver "talks" to the device it controls; this communication can range from simple manipulation of certain registers on the device's hardware interface to sophisticated messaging protocols. Message-based protocols usually involve the translation of a standard OS-based protocol, such as SCSI or ATA, to an independent-hardware-vendor-supported messaging protocol that the device's firmware or hardware understands. An example for a storage driver would be translating a SCSI I/O request from the SCSI subsystem of the kernel to an independent-hardware-vendor-specific messaging mechanism.

A device driver may also need to support custom I/O control or similar management mechanisms that the end user employs to manage the hardware. For example, to update the firmware on a device, the device driver would need to provide a mechanism to pass custom commands to the device that are—and must be—OS-agnostic. Modern device

drivers do robust error checking and use sophisticated methods to detect and recover from errors; this feature is especially true of storage and RAID (redundant-array-of-independent-disk)-related products. In addition, to enhance usability, the device driver often translates cryptic error and status codes from the firmware to human-understandable formats.

All of these functions in a device driver are device-specific, so does a driver designer need to rewrite the driver for each new OS that it will support? CDL is a "write-once, run-anywhere" mechanism that enables a designer to cleanly, rapidly, and with the least overhead write the driver once and carry it to a new OS, even to an embedded environment.

The CDL layer implements device-specific functions in an OS-agnostic manner. It abstracts the device-specific layer, and it accesses the device via the CDHI and CDHS through a well-defined API. A design team can avoid reimplementing the entire driver or porting it over with significant costs when adopting a different OS by writing the CDHI and CDHS layers. This task is relatively easy for a reasonably seasoned device-driver developer with the aid of the OS-kernel documentation or driver-development kit.

The task of encapsulating the device-driver intelligence into an OS-independent layer is more complex than it sounds. To gain the benefits of using a CDL, the driver-design team should comprise a group of cross-platform driver experts.

When attempting to use a CDL approach to creating device drivers, it is important for the driver designer to understand how each OS that the CDL supports works at a kernel level. This knowledge will influence the CDL architecture and is necessary to effectively partition the CDHI and CDHS interfaces to bar any OS-specific functions from the CDL. For example, the CDHI- and CDHS-component interface for a Microsoft Windows storage-device driver (typically, a miniport) would have to interface with the Microsoft-port-driver interface so that the CDL does not directly interface with the Windows storage stack (**Figure 2**). The same example using a Linux storage subsystem represents no change for the CDL, but the CDHI and CDHS components work with different OS-driver interfaces from those in a Windows environment (**Figure 3**).

One of the core responsibilities of an OS is to provide synchronization and locking capabilities for a kernel-mode driver. This function allows portions of a driver to run at the same time as other portions or to ensure that only one portion of a driver can execute at any time. In Windows, a typical storage miniport driver has minimal control over the synchronization of starting an I/O versus handling I/O completion in the interrupt-service routine. In a SCSI port miniport model, these activities are mutually exclusive, whereas the newer Storport miniport model improves on this feature by allowing separate locking for building an I/O, queuing an I/O to the controller, or completing an I/O using a simplified spin lock and deferred procedure-call interface.

Linux, on the other hand, gives the driver writer complete control over the use of spin locks and semaphores to control driver synchronization. The widely differing approach these operating systems take to synchronization can complicate the design of a CDL if the CDL code itself enforces locking and synchronization. To simplify the design, a designer may choose not to implement locking and synchronization in the CDL itself but to rely on a set of constraints that force the CDL to hand over the locking and synchronization to the CDHI component.

A good rule of thumb is to make all of the CDL interfaces non-reentrant, to make them run to completion, and to force users of the CDL to enforce this constraint. Another possibility is to include certain classes of CDL interfaces that adhere to different constraints, such as using the routines add_request_to_queue() and remove_request_from_queue(), which might be mutually exclusive of each other but can execute at the same time as other CDL API.

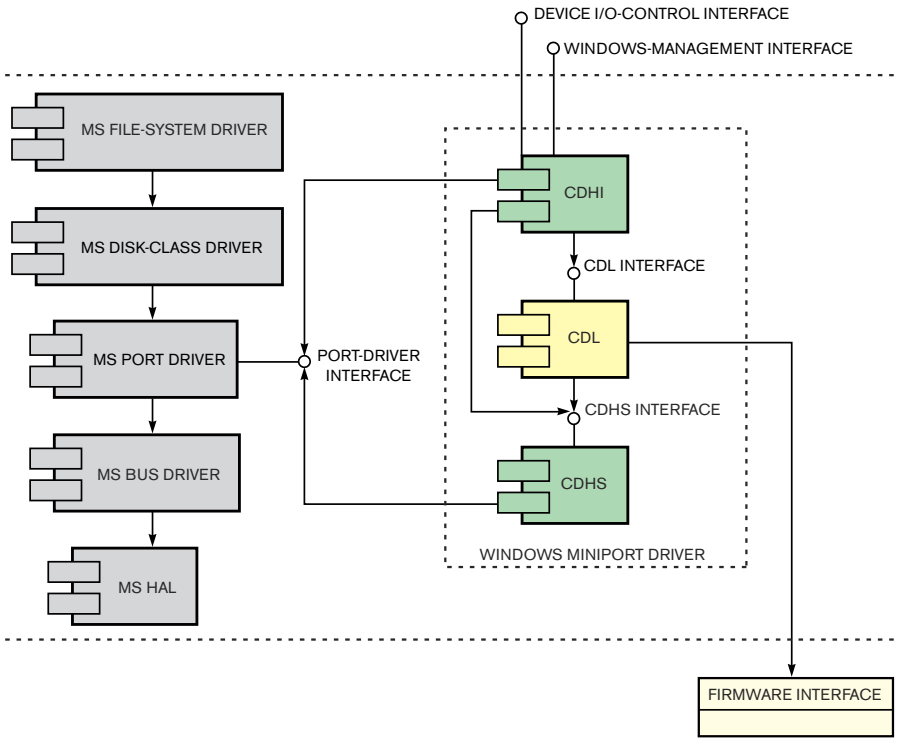


Figure 2 The CDHI- and CDHS-component interface for a miniport in a Windows storage subsystem would have to work with the Microsoft-port-driver interface so that the CDL does not directly interface with the Windows storage stack.

THE DATA DETECTIVE

Mind Your I's and Q's

Most people who use cell phones, portable PCs, and other wireless devices understand the benefits of radio-frequency communications. Because consumers always expect more capabilities, designers must push communications to higher frequencies, use more sophisticated information encoding or modulation schemes, and transmit or receive at lower power. Often they require higher data throughput or higher bandwidths. Engineers refer to bandwidth rather loosely, though, which can cause confusion. Keep in mind two different types of bandwidth: A WLAN based on IEEE 802.11g, for example, provides a data bandwidth as high as 54 Mbits/sec. In the US, those transmissions take place between about 2.412 and 2.462 GHz, a signal bandwidth, or frequency range of about 50 MHz.

By modulating a carrier signal, we add information that others can receive and demodulate. There are three parameters of a signal that can be modified to convey information: amplitude, frequency anad phase.

In mathematical terms, think of modulation as:

$$\text{Signal} = A_c \cos(2\pi f_c t + \phi)$$

Where A equals amplitude, $2\pi f_c t$ equals frequency, and ϕ equals phase. The combined frequency and phase terms govern the "angle" described by the cosine term (Figure 1). Thus, by independently changing two components of a signal—its amplitude and its angle—you can increase a signal's information-carrying capacity and its immunity to noise beyond that of basic AM, FM, or PM signals.

Digital-communication techniques specify a set number of "states" for each type of digital modulation. A signal that employs 32-state quadrature amplitude-modulation (32 QAM), for example, allows 32 signal variations. Each variation conveys five bits of information ($32 = 2^5$). Instead of modulating phase and amplitude, the QAM technique modulates the *amplitude* of an in-phase carrier (I) and the *amplitude* of the carrier shifted one quadrant (Q), or 90 degrees (Figure 2). Combining the modulated I and Q signals produces a single signal in which the orthogonal I and Q components do not interfere with one another. Engineers have found it easier to modulate and demodulate the amplitude of two signals than to change the amplitude and phase of one signal. (An upconverter mixes the modulated baseband signal with a high-frequency signal to create the final RF transmission signal.)

A receiver splits the I and Q information, which in raw form looks like a Cartesian plot, often called a "constellation" diagram (Figure 3). Each dot represents one of the 32 values allowed in a 32 QAM signal. Think of the "vector" as a line that connects the origin and any dot. Note the relationship between I/Q and magnitude and phase. Because the combined I/Q signal produces a vector, engineers refer to instruments that generate and analyze I/Q-modulated signals as vector signal generators (VSG) and vector signal analyzers (VSA).

Test Your IQ

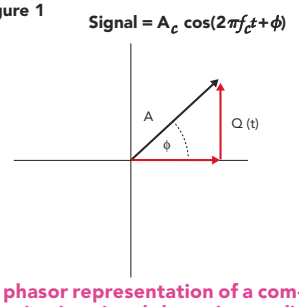
Jill has designed a circuit that demodulates a 32 QAM signal. When she looks at the data stream, though, she sees what seem like random bits—more like a noise signal than data.

Can you help Jill measure and analyze the signals to determine what has gone wrong?

http://rbi.ims.ca/4402-503

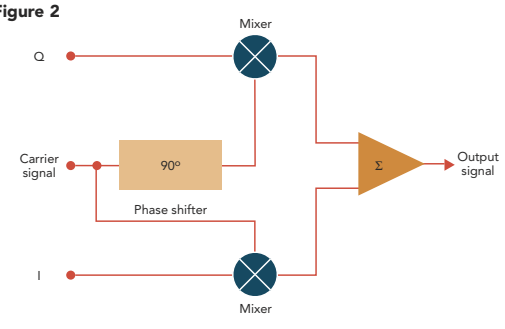
RF communications cannot occur without errors. So during vector analysis of communication signals, engineers quantify a modulation-error ratio (MER) and an error-vector magnitude (EVM). Both of which require acquisition of signal data, comparison with known-good data, and calculation of results. In short, MER calculates the peak or the rms value of the error vector between the ideal vector and the actual received vector for all points in a constellation diagram. EVM measures the difference between the ideal and the actual vector values in a transmission. Many vector signal analyzers can provide MER and EVM values, which help characterize the quality of a modulated signal.

Figure 1



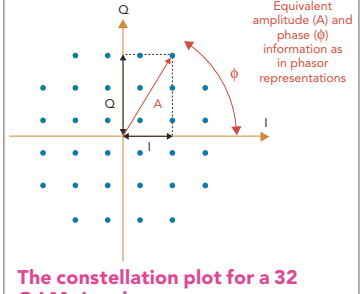
A phasor representation of a communication signal shows its amplitude and phase components.

Figure 2



A typical I/Q-modulation circuit.

Figure 3



The constellation plot for a 32 QAM signal.

Go to http://rbi.ims.ca/4402-503 to solve the challenge!

Another area in which operating systems vary considerably is memory management. Whereas most operating systems provide kernel facilities to allocate and free types of memory, such as kernel virtual, cache, and DMA memory, operating systems vary considerably in how and when they allocate the memory and how much memory is available.

In a typical Windows miniport environment, the OS must allocate most memory at driver-initialization time and not at runtime. The port driver allocates the DMA memory for building the I/O request and scatter-gather lists for DMA operations. The driver does this operation on behalf of the miniport and attaches the memory to each I/O it sends to the miniport for processing. Linux, on the other hand, allows the driver writer to allocate and free memory at any time during the driver execution.

To allow the CDL code to use these memory models, the code may leave memory allocation for I/O to the CDHI component, so that the CDL need not understand what OS is running and try to manage memory internal to the common code. This approach allows Windows and Linux to get the I/O memory in their unique way but to use of CDL to link the memory and the request. This approach also affects the CDHS component because the CDL code may need to allocate memory resources during runtime; in a Windows environment, this requirement may force the driver writer to allocate a single contiguous block of memory at initialization time and implement a page- or a slab-allocation/deallocation scheme to break that single block into more usable block sizes for the CDL.

Understanding the hardware the device needs to support is an obvious step for any device-driver designer. In some cases, the hardware may support a PCI-memory interface that a host-OS device driver typically uses; in an embedded-system application, the hardware may expose a local-bus memory interface. Because one goal of a CDL is to hide the underlying hardware details, if the driver must support multiple hardware platforms, the CDL designer may want to use separate components to manage this situation with a common interface that the rest of the CDL code can use. This approach allows the use of different hardware-specific modules without having to change other CDL components, and it allows the driver writer to create different flavors of the drivers with compilation-time build switches.

Understanding the protocols the device driver needs to support is another obvious step for a driver designer. If the hardware requires the use of one protocol for the SCSI controller and a different hardware protocol for the SATA controller, it might be advantageous to implement them as separate modules that have a common interface for use by other CDL components. Again, using compilation-time build switches allows a designer to change protocol-specific portions of the CDL without rewriting other portions of the CDL.

Once a designer understands these and a host of other, less significant constraints, the architecture of the CDL can become a modular design that potentially allows the designer to selectively compile multiple hardware-bus interfaces and protocols into or from the library, allowing for flexibility and extensibility.

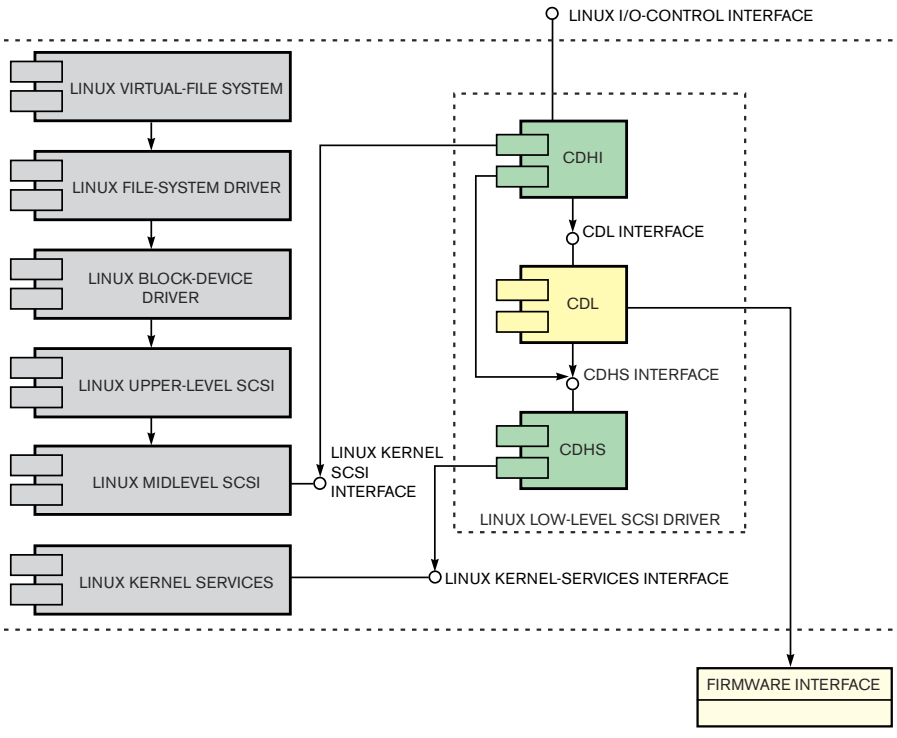
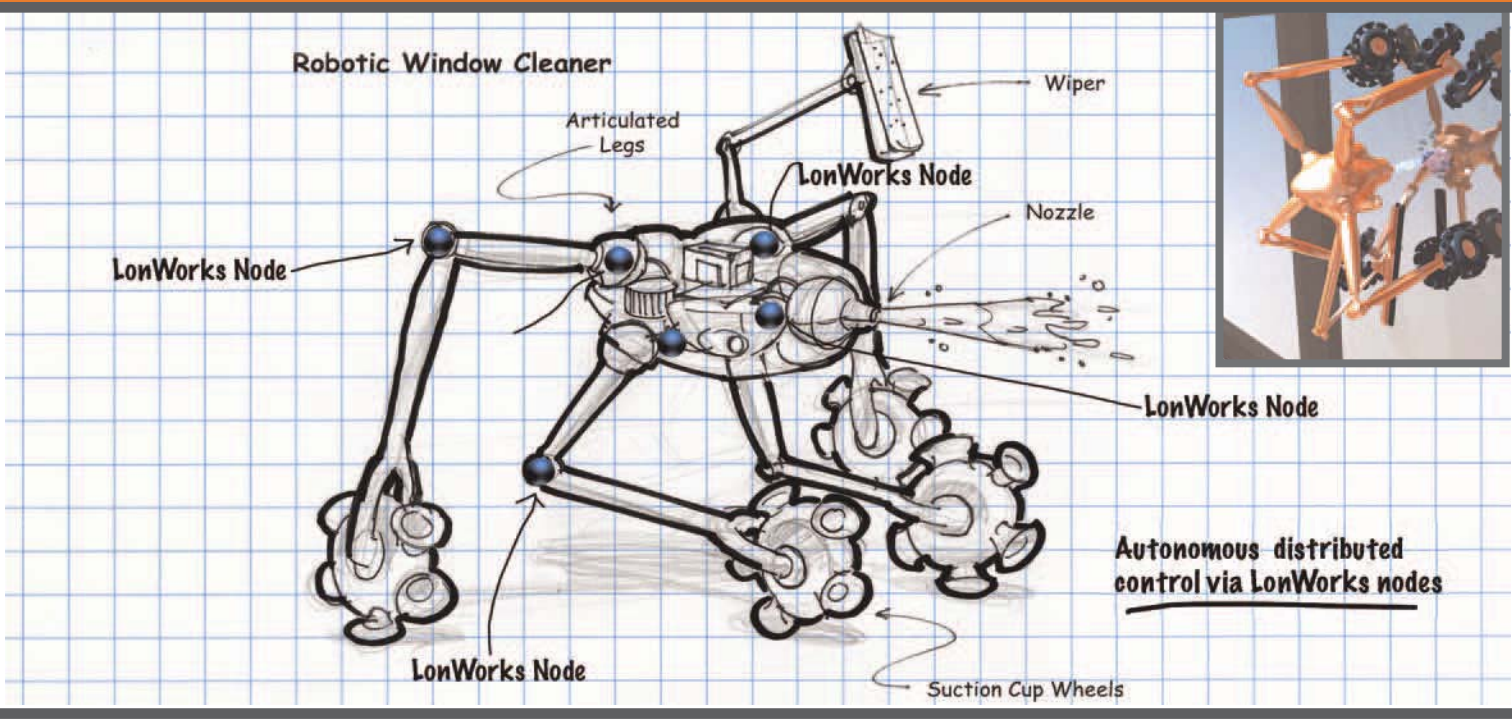


Figure 3 The CDHI and CDHS components for a Linux environment work with different OS-driver interfaces from those in a Windows environment.

ARCHITECTURE DETAILS

Figure 4 illustrates a possible CDL architecture that embodies some of these features. The resulting CDL code divides into a number of managers that compartmentalize groupings of functions. Starting at the bottom of the diagram, a local-memory bus and PCI-bus module allow the CDL to support an embedded version that a RAID-on-chip or storage appliance might use or to support a traditional host-OS device driver through an exposed PCI memory-mapped interface. To hide the potential difference between hardware interfaces, a bus manager resides atop the local- and PCI-bus components. This approach provides a consistent interface for the protocol components and any other higher level components that will use the hardware interface.

The transport-interface-manager module would use the bus-manager interfaces to implement the transport-firmware interface that a ven-



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dor's product uses. This module does the "heavy lifting" in the CDL and provides an OS-independent transport interface that high-level components can use. In this example, a protocol manager sits on the transport-interface manager; this protocol manager handles SAS-, SATA-, and Fibre Channel-protocol-specific tasks, allowing them to use the transport-interface manager. The functions might include target-device discovery and rediscovery, protocol-specific asynchronous messages, and error handling.

Other high-level components, such as the configuration-manager component, sit on top of the protocol manager. The configuration manager serves as a data-storage area for configuration parameters that all CDL components use. Also above the protocol component, a target manager provides a common set of interfaces for discovering target devices, consistently mapping the target devices, and to potentially handle target-level resets and I/O aborts. An I/O-control manger provides a consistent set of high-level interfaces for management applications. A CDL component ties together all of the individual components and provides interfaces for other functions.

The proposed architecture suggests that the driver must traverse many layers of interfaces in the important I/O-performance path, but the designer can minimize the CDL-code overhead by providing an interface directly into the transport-interface manager to bypass most of the CDL components. Likewise, a designer can minimize the I/O-completion path by using a CDHS callback directly from the transport-interface manager to bypass other components and to improve performance. A designer can also minimize the layers below the transport-interface-manager module. In most cases, a designer can use a compilation-time macro substitution for the bus-manager layer whether using the PCI-manager or local-bus-manager components. The CDHS interfaces could also use a macro substitution that would place the calls inline and avoid the extra overhead of C-function calls for these interfaces.

To facilitate the use of the CDL on many operating systems, the CDL, CDHI, and CDHS components should use a common types.h header file that defines all of the data types in an OS-independent manner. If the designer has correctly built the CDL code, this header file should be the only CDL file that will need OS-specific additions for each OS.

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PROS AND CONS

Independent hardware vendors face the challenge of supporting many operating systems; this requirement was the primary motivation for developing a CDL. The need to develop, maintain, validate, and support device drivers for the various host- and embedded-system environments makes these tasks increasingly complex. With a CDL approach, the vendor can experience significant savings, leading to a shorter time to market.

The CDL is portable and can move to different environments with minimal changes. Intel has successfully ported a CDL not only to different hosts and embedded environments, but also to user applications. With the CDL architecture, it is relatively easy to support a new operating environment. This process involves developing the CDHI and CDHS portions, which the appropriate operating-environment specialist can easily do. If the driver designer can build enough flexibility into the CDL design, it is relatively painless to reconfigure the code base into a CDL "lite" version. An embedded-system with size limitations and high performance requirements could then use this version.

A related benefit is CDL extensibility, which depends on the internal design of the CDL itself. Adding a new function translates into adding a new functional manager that accomplishes the task and interfacing it with the other managers. The complexity of this task depends on how pervasive the new feature is. For example, adding a new I/O bus would involve adding a subcomponent to the bus manager in the CDL. This task is easier than adding a new configuration parameter that would impact all the managers.

Implementing a test strategy that employs the modularity of the CDL architecture can significantly reduce the testing cycles for device drivers for multiple operating environments. Designers can simultaneously test the CDL across multiple environments and distribute test coverage among them. Bugs in the CDL should appear in any environment using the CDL-based driver. Regression testing also becomes easier if the designer updates only the OS-dependent portion of the driver code base.

In addition to rapid development of drivers, the CDL architecture enhances the maintainability of the driver code because most of it is now common. It is easy to maintain this code base rather than manage diverse driver-code bases. With the shorter testing cycle, the

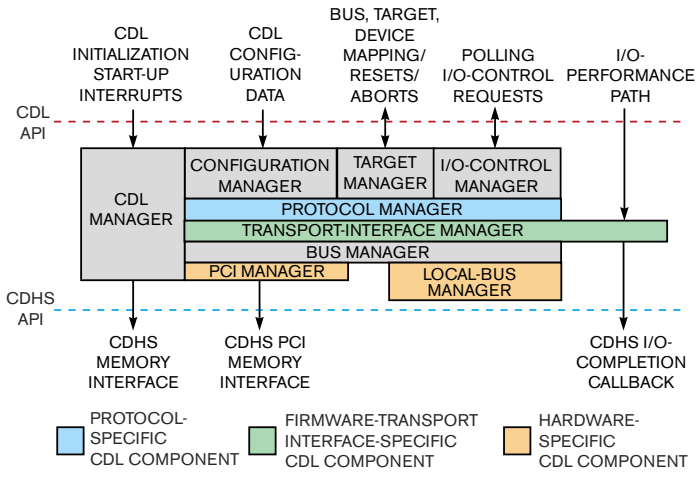

Figure 4 A possible CDL architecture embodies CDL code that divides into a number of managers that compartmentalize groupings of functions.

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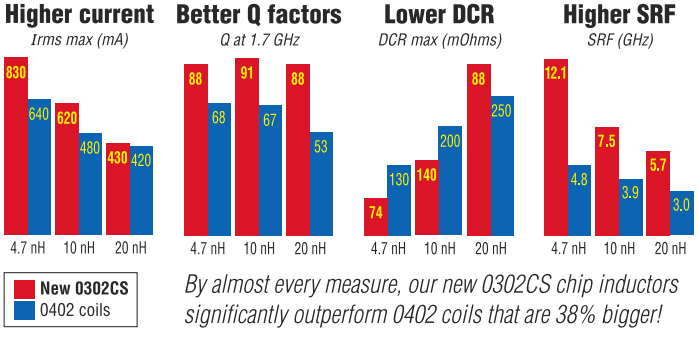

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CDL architecture also provides the advantage of having to fix bugs only once in the common portion even if the bug existed across multiple operating systems. A company can save a significant amount of time in testing and validation.

A typical implementation vertically partitions device-driver development teams, according to the operating environment for which they develop. This increase in developer and tester resources, in the form of OS experts and domain specialists, grows exponentially with the addition of each operating environment. Little interaction or cooperation occurs among the teams, leading to inefficient use of resources, because each team duplicates the effort necessary for going through a product's life cycle. The requirements, design, and development for each driver are usually distinct and varied. This disparity becomes more visible during the maintenance phase of the driver. Teams duplicate efforts to find, characterize, and resolve bugs within each vertical segment. With CDL, an organization can have just one device-driver team comprising at least one hardware/firmware-domain specialist and at least one operating-environment expert, providing for a cross-functional driver-development team.

Despite the benefits of the CDL architecture, it is not without pitfalls. An obvious one is the concern regarding the performance penalty designers incur due to the level of abstraction CDL introduces into the driver. The driver-development team can minimize this drawback by taking extreme care when designing and implementing the CDL components. Another potential issue with a CDL is the kind of licensing the developer chooses for the CDL component. If you have one or more operating environments with conflicting license requirements, a problem may arise. Most organizations face misconceptions and fears regarding mixing open- and closed-source code. One possible approach is to license the CDL under both a commercial and a compatible open-source licensing scheme. But each organization needs to determine its own needs and work out the details with its legal department. EDN

AUTHORS' BIOGRAPHIES

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1 Topology for high current
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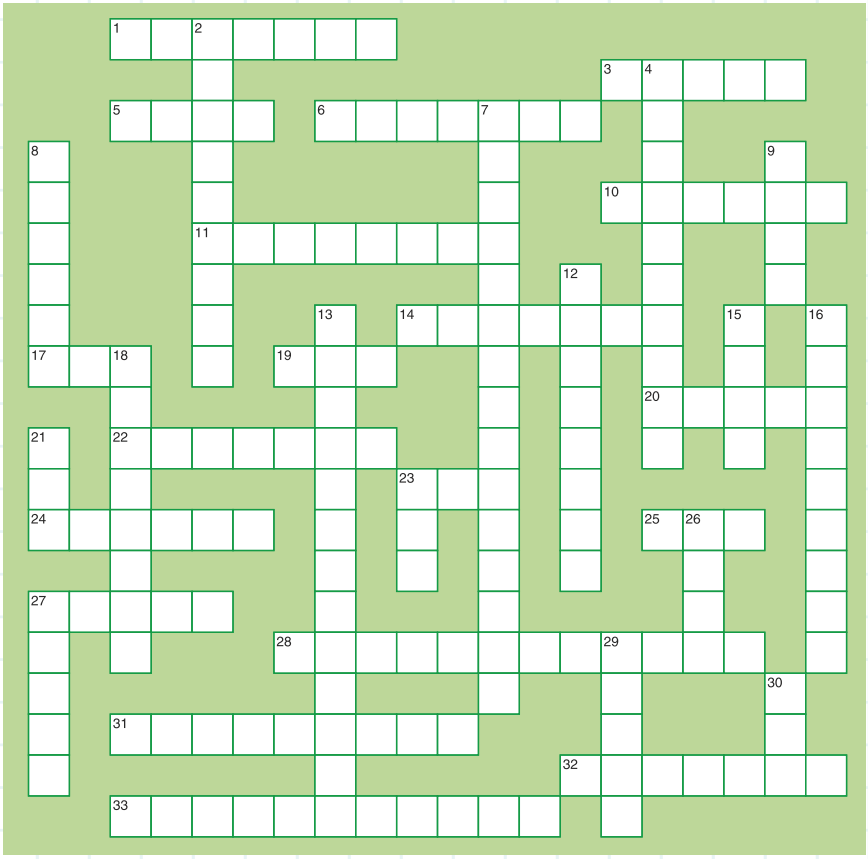
6 Noise, but you can't LISN for it
10 AC-DC conversion technology, not efficient
11 Information from the front
14 Inductance, not coupled
17 Dissipative capacitor parasitic
19 1000s inverted time
20 Limits voltage spike after switching
22 Secondary source of supression
23 Unwanted, but best not allowed to leave
24 Specified by $R_{DS(ON)}$
25 802.3af
27 PN, connected
28 *TinySwitch*® operating principle
31 Blocks DC
32 Efficient and simple SMPS topology
33 The best control scheme for multiple output designs



DOWN

2 Turns AC to DC
4 What the doe's star seeks
7 Power reservoir
8 Ground for the low side
9 A powerful Scottish gentleman
12 A 50% enthusiastic goodbye
13 Reduces electrostatic coupling in transformers
15 An AC path from primary to secondary
16 The original high-voltage integrated switcher IC
18 _____ values sum in series
21 A Top regulation method
23 External Power Supply
26 Communicates with itself at a required distance
27 Electron sink
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BY DAVID TORMEY • COPLEY CONTROLS

Using PWM servo amplifiers in noise-sensitive applications

DIGITAL PWM SERVO AMPLIFIERS ARE SMALLER, MORE EFFICIENT, LESS EXPENSIVE, AND EASIER TO USE THAN THEIR LINEAR COUNTERPARTS.

A motor-drive servo amplifier's output voltage has a fundamental frequency and amplitude that corresponds to the motor speed, torque, and number of motor poles. PWM amplifiers, by their nature, also produce higher frequency voltage components that mainly correspond to the PWM rise and fall times and repetition rate. The fast edges that appear on the PWM output can capacitively couple noise currents to nearby conductors unless the system designer takes steps to reduce or eliminate coupling paths.

Designers must take care, therefore, when designing PWM amplifiers in noise-sensitive applications. Noise-sensitive applications include those that use high-resolution encoders, ultrasonic transducers, or other low-level, medium-frequency signal producers. Grounding, shielding, and other circuit-design techniques mitigate most noise problems. The most noise-sensitive applications may require additional noise-reduction methods, such as PWM edge filters. Simple design guidelines ensure effective management of capacitively coupled currents and help you to reap the full range of benefits that PWM servo amplifiers offer.

PWM APPROACH

PWM encodes analog signals within a digitally compatible, bi-level pulse train. Variations of PWM exist, but servo amplifiers most commonly use varieties with a constant carrier frequency. Typical PWM carrier frequencies for servo amplifiers are 10 to 20 kHz. Variations in the pulse width encode the analog-signal information in the PWM pulse train. For fixed-frequency PWM, designers sometimes describe the pulse width in terms of duty cycle: the ratio of the pulse width to the PWM period.

In the frequency domain, the PWM drive voltage has two primary frequency components. The first is the fundamental motor-drive component, which corresponds to the motor speed and number of motor poles. This fundamental component creates the torque-producing motor current. The second frequency component is at the PWM carrier frequency. Because this voltage does not correlate with the fundamental motor-drive frequency, any current that the PWM component of the motor-drive voltage produces does not contribute to motor operation. Any current at this frequency only creates power loss in the motor. Fortunately, the PWM frequency is typically high enough that the motor's inductive impedance is large at the PWM frequency. Because current equals the voltage divided by the impedance, the current at the PWM frequency is usually small.

The primary motivations for using PWM motor drives are size reduction and efficiency improvement. The IGBTs (insulated-gate bipolar transistors) or power MOSFETs that convert the dc input voltage to a motor-drive voltage operate most efficiently when they operate as switches. The PWM signal drives the IGBTs or MOSFETs either fully on or fully off with rapid tran-

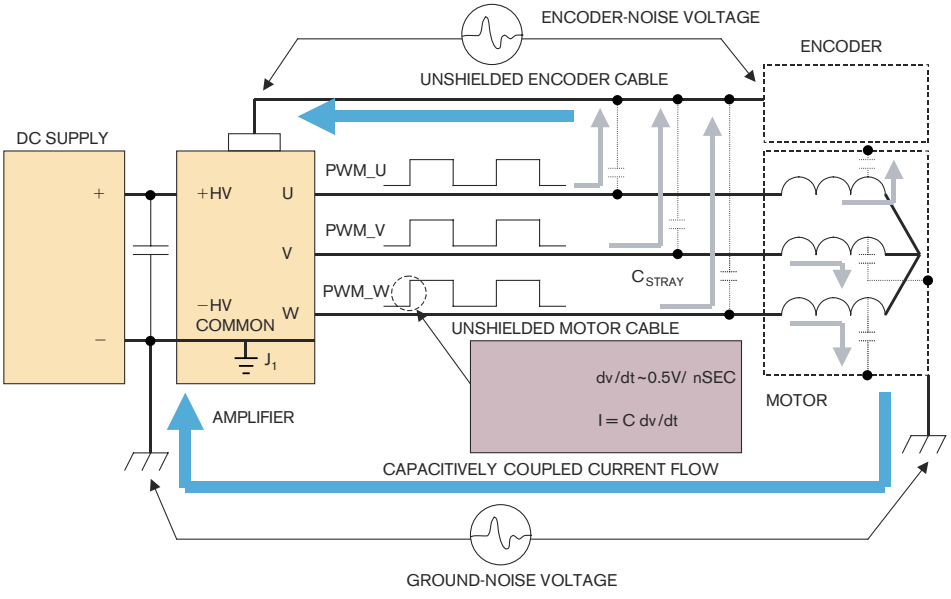

Figure 1 Drive-signal edges capacitively couple noise from unshielded cabling to other signal leads, such as those that carry shaft-encoder information.

sitions between the two states. In linear amplifiers, these devices operate in their linear region, and, as a result, the drive amplifier's power losses and overall size are larger.

CAPACITIVE COUPLING

While the transistors are switching between their on- and off-states, they pass through their linear region and dissipate energy. The faster the transistors switch, the less energy they dissipate, and the more efficient the amplifier is. If high efficiency were the amplifier design's sole requirement, the goal would be to as quickly as possible switch the transistors. There is a trade-off, however. The high dv/dt that accompanies rapid switch transitions can couple noise onto nearby circuits. In general, faster switching translates into higher noise levels. The amplifier designer must strike a compromise, then, between efficiency and noise levels.

The noise couples through the parasitic capacitance between the motor-cable conductors and the adjacent circuits (**Figure 1**). The **figure** shows a generic servo-motor application with a dc-powered PWM servo amplifier driving a brushless motor. The amplifier receives position feedback from an incremental encoder. In this example, neither the motor cable nor the encoder cable is shielded.

The amplifier PWM output-voltage waveforms on phases U, V, and W are in-phase, and their duty cycle is 50%. This in-phase and duty-cycle condition is typical when the system is holding position; the motor current and speed are near zero. The lower half of the **figure** shows a detailed view of a rising edge on the phase W output. Note

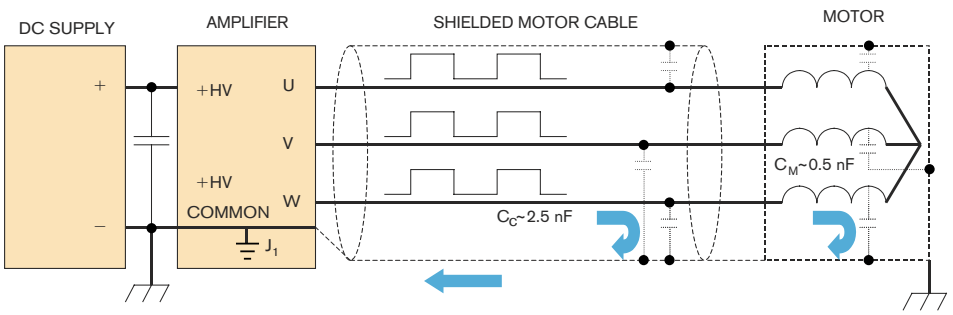

Figure 2 Shielding the drive cable safely shunts the noise currents to ground.

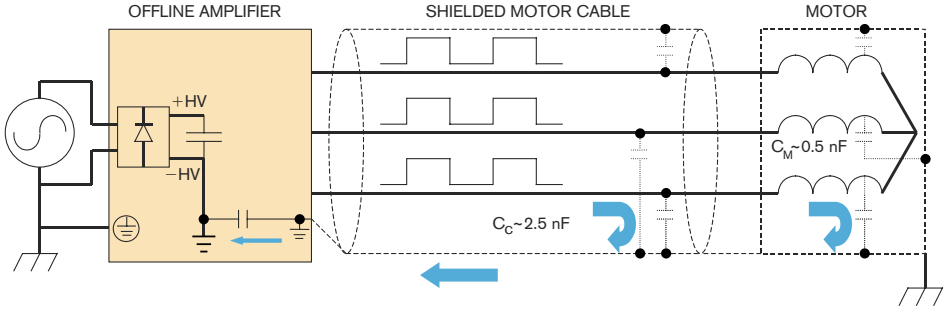

Figure 3 An offline-powered amplifier's negative supply is not directly available as a return path for noise currents. Instead, a high-voltage capacitor internal to the amplifier must shunt the negative supply rail to earth ground.

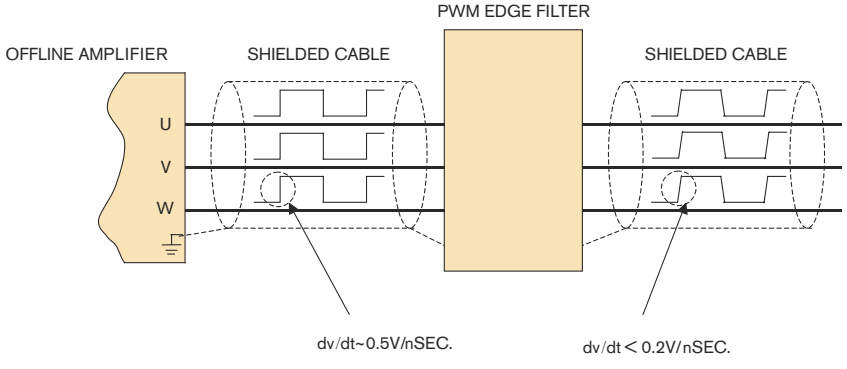

Figure 4 Edge filters reduce the drive signal's dv/dt and thereby attenuate the noise at its source. The extent to which you filter, however, is a compromise between noise reduction and overall drive efficiency.

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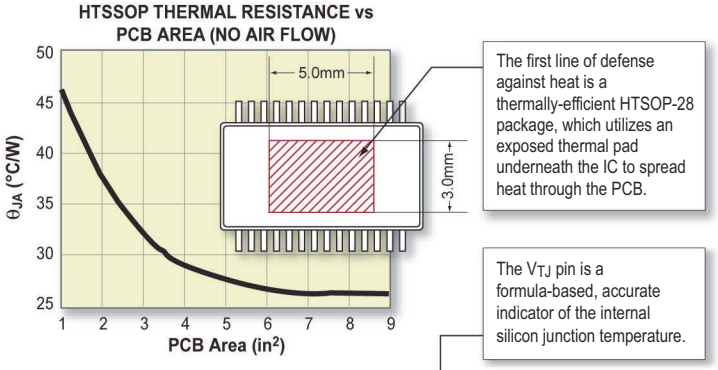

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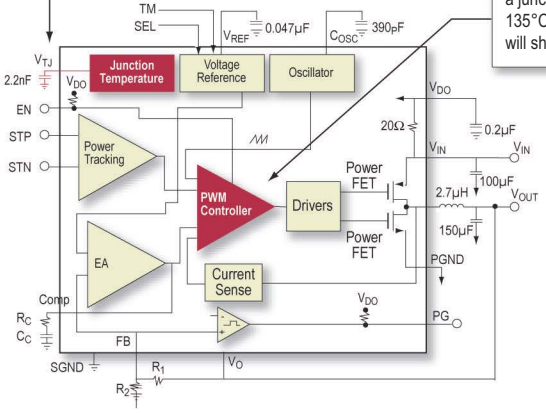

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that this edge has a finite rise time; a typical dv/dt is on the order of 0.5V/nsec. Below this rising-edge detail is a waveform showing the shape of the noise-current coupling through the parasitic capacitance to adjacent circuits as a result of the PWM rising edge.

The size of the parasitic capacitance between the motor conductors and an adjacent conductor depends on the size, shape, orientation, and proximity of the adjacent conductors. The equation I=C dv/dt calculates the amount of noise current that flows, where dv/dt is the rate of change of PWM voltage, and C is the value of the stray capacitance. Whether this noise current causes circuit-function problems depends on the exact path it follows and the sensitivity of adjacent circuits.

The noise current returns to its source, the amplifier, by the path of least impedance. For the frequencies generated by the PWM edges, this path usually means the path of least inductance. In the case of a system without any shielding in place, the path of least impedance is not well-defined. The noise currents may flow in nearby conductors, such as encoder cables and other circuits that have a common circuit ground with the amplifier. When these currents flow in encoder wires, a voltage develops between the encoder and the amplifier ends of the wire. If this voltage is large enough, the amplifier's encoder-receiver circuit falsely detects or masks a true encoder transition, resulting in a missing or an extra encoder count. Similarly, these noise currents can develop voltage drops across ground conductors and thereby introduce noise on other signal lines.

The noise currents are largest when the motion-control system is holding position. The rising and falling edges of all three waveforms coincide in this condition. The current spikes that result from the PWM edges thus all occur at the same point in time. The net peak current that capacitively couples to external circuits is then the sum of the individual currents contributed from the U, V, and W phases. On the other hand, when the motor is moving and producing torque, the PWM duty cycle of each phase changes, and the rising and falling edges no longer coincide. In this condition, the current spikes appear at a higher frequency but with lower amplitude.

THE SHIELD DOES NOT ELIMINATE BUT RATHER CONTROLS CAPACITANCE SO THAT THE COUPLING TERMINATES AT THE SHIELD AND NOT AT THE EXTERNAL CIRCUITS.

MANAGING CAPACITIVELY COUPLED CURRENTS

You can reduce problems related to capacitively coupled PWM noise by using cable shields and proper grounding techniques. There are two main objectives of grounding and shielding. The first is to force the capacitively coupled currents to flow in a well-defined path; the second is to ensure that any noise voltage developed across that path does not disturb critical signals. A motor-cable shield connected to both the motor frame and the amplifier ground establishes a controlled path through which capacitively coupled currents flow (**Figure 2**). The shield does not eliminate but rather controls capacitance so that the coupling terminates at the shield and not at the external circuits. The ideal overall shield, enclosing all three conductors, provides 100% coverage and a zero-impedance path for the high-frequency noise currents. A zero-impedance path ensures no voltage drop along the shield and that the entire shield is at the high-voltage-common potential.

TABLE 1 RECOMMENDED GROUNDING AND SHIELDING PRACTICES

Recommendation	Comments/rationale
Keep motor cables as short as possible.	Capacitance is a function of cable length whether or not a shield is used. Keeping cables short minimizes capacitively coupled currents.
Use a motor cable with a high-quality shield.	The best shield provides complete coverage of the enclosed conductors and is also a good, high-frequency conductor. A combination braid-and-foil shield is best but not necessary for all applications.
At the motor end of the cable, make a low-impedance connection between the shield and the motor frame.	If the motor has a metal shell connector, then you can tie the shield directly to the metal shell of the mating connector. Otherwise, the connection between the cable shield and the motor frame should be as short as possible.
At the amplifier end of the cable, make a low-impedance connection between the shield and the amplifier's common potential for nonisolated, dc-powered amplifiers only. For offline-powered amplifiers, connect the shield to the chassis ground.	The connection should be as short as and have the lowest inductance possible. In the case of pc-board-mounted amplifiers, the pc-board trace from the shield to the amplifier's common should be short and wide. Also, the connection should be directly to the positive-high-voltage common at the amplifier power connector.
Avoid running sensitive signal cables, such as encoders, small signal transducers, and others, in the same cable bundle with the motor cable.	Capacitive coupling is a function of proximity. Separating sensitive signals from the motor cable reduces capacitive coupling to the sensitive signals.
Use shielded cable for the sensitive signals. Connect this shield to the high-voltage common only at the amplifier end for nonisolated, dc-powered amplifiers only. For offline-powered amplifiers, connect the shield to the chassis ground.	The overall shield on the motor cable should prevent coupling to sensitive signals. An overall shield on cables with sensitive signals provides a second line of defense.
Add capacitance across the high-voltage dc bus to keep switching currents local to the amplifier.	The PWM switching also draws transient currents from the dc supply. For some amplifier models, additional capacitance connected to and close to the amplifier's positive-high-voltage and positive-high-voltage common terminals is recommended. Refer to the amplifier data sheet for details.
Refer to the amplifier data sheets for model-specific considerations regarding wiring best practices.	Each PWM amplifier model has noise-related characteristics depending on the amplifier topology and basic construction—pc-board-mount amplifiers versus panel-mount types, and offline versus dc-powered, for example.

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LT1766	5.5V to 60V	1.25A	Buck Converter	140	TSSOP-16E
LT1976	3.3V to 60V	1.25A	Buck Converter	140	TSSOP-16E
LT1936	3.6V to 36V	1.4A	Buck Converter	150	MSOP-8E
LTC®3803-5	6V to 72V	3A	Flyback Controller	150	ThinSOT™
LTC1772	2.5V to 9.8V	5A	Buck Controller	140	ThinSOT
LTC3731	4.5V to 36V	60A	Sync Buck Controller	140	SSOP-36

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The shield connection to the motor frame terminates the capacitive coupling between the motor windings and motor frame. In this way, the motor frame provides an overall shield for the motor windings. The cable shield provides a path for these currents to return to the amplifier's common, as well.

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Typical values for shielded-cable capacitance and motor-winding-to-frame capacitance are on the order of 250 pF/ft and 0.5 nF, respectively. The cable capacitance is a measured value for four #16 AWG conductors with a foil shield. If you use a PWM rising-edge rate of 0.5V/nsec, the peak current flow in the overall shield is I=Cdv/dt=(2.5 nF+0.5 nF)0.5V/nsec=1.5A peak. On the PWM falling edge, the same calculation holds, except the polarity of the current is reversed. So, when the motor is just holding position, you could expect a peak current of 3A p-p flowing in the cable shield. **Table 1** presents recommendations for grounding and shielding practices.

EDGE FILTERS

An offline-powered amplifier takes ac power from the mains and uses an internal rectifier to supply a dc bus (**Figure 3**). The negative side of the dc bus is not available for connection to the motor-cable shield, as is the case with nonisolated dc-powered amplifiers. In this topology, the bus is typically 100V or more below earth-ground potential, and connecting the cable shield to this potential would constitute a safety hazard.

Nonisolated, dc-powered amplifiers operate from line-isolated dc-power supplies; the negative rail of these supplies commonly connects directly to earth ground. In such arrangements, connecting the cable shield to the common bus is safe, practical, and effective.

In the case of the offline-powered amplifier, the shield connects to the amplifier chassis ground. A high-voltage, safety-rated capacitor internal to the amplifier bypasses the bus to chassis ground. This connection provides a path for the noise currents flowing in the shield to return to their source—the bus.

Offline-powered amplifiers usually operate from higher voltages than dc-powered amplifiers, and, as a result, the dv/dt of their PWM outputs tends to be higher than that of dc-powered amplifiers. Furthermore, because the cable-shield currents flow through the internal capacitor before returning to the bus of the amplifier, cable shielding tends to be less effective than in the dc-powered arrangement. These facts make PWM noise issues more difficult to address in systems using offline-powered amplifiers.

For noise-sensitive applications that use offline-powered amplifiers, you can use another noise-abatement tool: the PWM edge filter. PWM edge filters use passive components to reduce the dv/dt of the amplifier PWM edges (**Figure 4**).

The PWM edge filter connects in series between the amplifier and the motor and increases the rise and fall times of the PWM edges. The edge filter reduces the peak amplitude of all capacitively coupled currents. Again, there is a trade-off in edge-filter design between overall efficiency and filter effectiveness. Filter designs that reduce the rise and fall times by an order of magnitude or more are too large and dissipate too much power. Edge filters that provide a more modest reduction in rise and fall times are effective in real-world applications. The example in the **figure** depicts the effect of a practical edge filter in which the dv/dt decreases from 0.5 to less than 0.2V/nsec. The noise current decreases by the same factor: I=Cdv/dt=(2.5 nF+0.5 nF)×0.2V/nsec=0.6A.

To maximize the edge filter's effectiveness, locate it as close to the amplifier as possible. Shield the section of cable connecting the edge filter to the amplifier and make it as short as possible. Maintain the shield on the section of cable between the edge filter and the motor and ensure continuity between the shields of each cable section. EDN

AUTHOR'S BIOGRAPHY

David P Tormey is senior design engineer at Copley Controls Corp (Canton, MA), where he designs PWM amplifiers and accessory products. He received bachelor's and master's degrees in electrical engineering from Worcester Polytechnic Institute (Worcester, MA). In his spare time, he enjoys running and travel.

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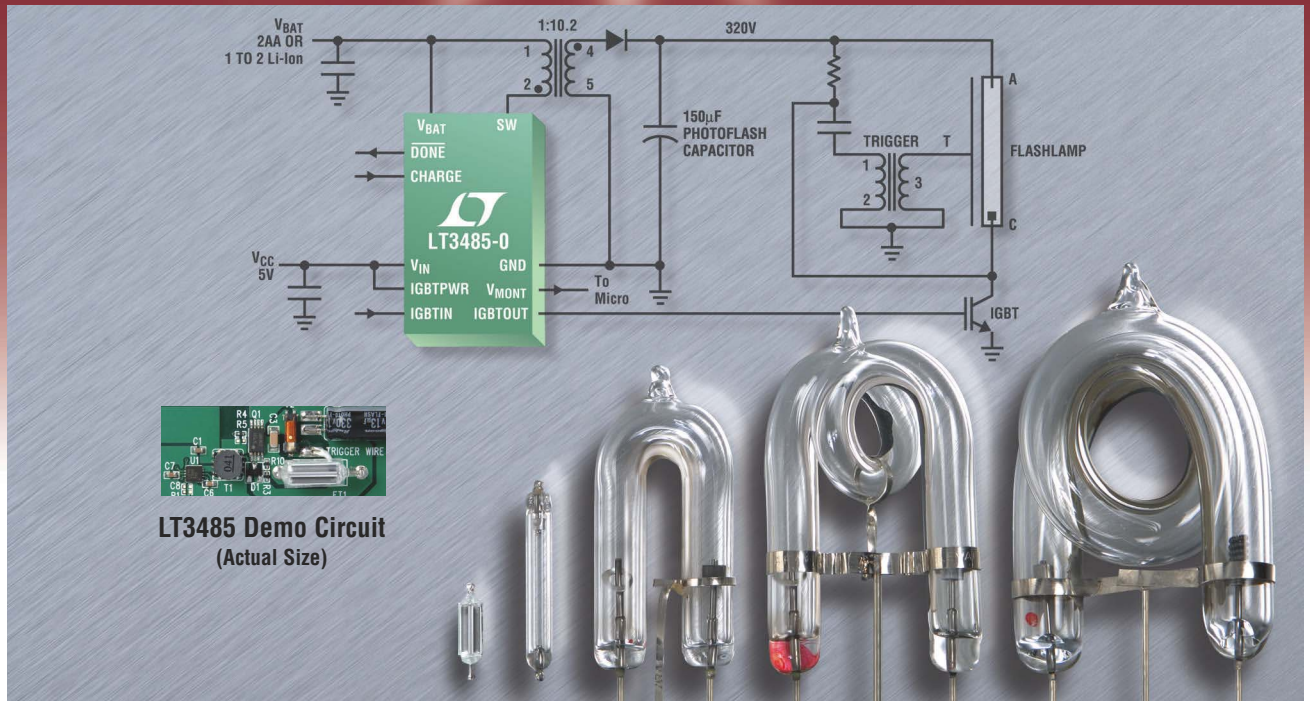

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LT3750	3V to 24V	Up to 4A*	MSOP

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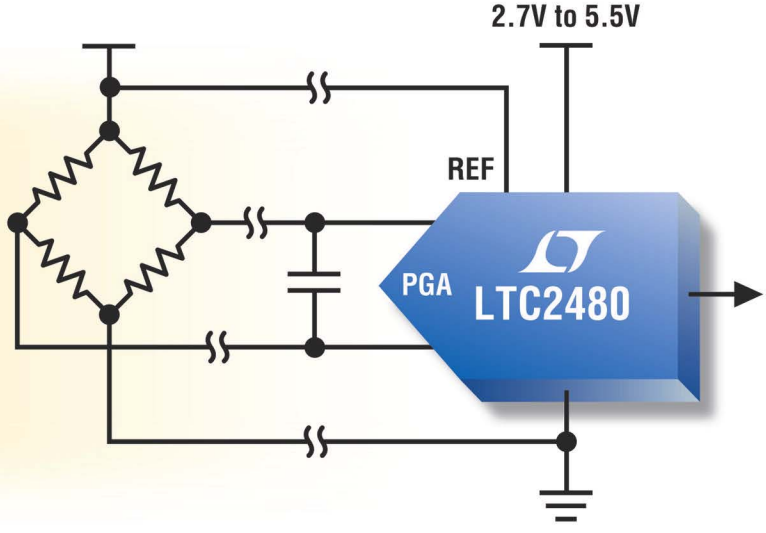

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LTC2482	16-Bits	SPI	1		7.5Hz	3mm x 3mm DFN-10	$1.65
LTC2483	16-Bits	I²C	1		7.5Hz	3mm x 3mm DFN-10	$1.65
LTC2484	24-Bits	SPI	1	Yes	7.5Hz/15Hz	3mm x 3mm DFN-10	$2.45
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DESIGN NOTES

Isolated Converters Have Buck Simplicity and Performance

Design Note 377

Kurk Mathews

Buck converter designers have long benefited from the simplicity, high efficiency and fast transient response made possible by the latest buck controller ICs, which feature synchronous rectification and PolyPhase® interleaved power stages. Unfortunately, these same features have been difficult or impossible to implement in the buck converter's close relative, the forward converter, often used in isolated industrial and telecom applications. That is, until now. The LTC®3706 secondary-side synchronous controller and its companion smart gate driver, the LTC3725, make it possible to create an isolated forward converter with the simplicity and performance of a buck converter.

Simple Isolated 3.3V, 30A Forward Converter

Many isolated supplies place the controller IC on the input (primary) side and rely on indirect synchronous rectifier timing and optoisolator feedback to control the output (secondary). The circuit shown in Figure 1 offers a more direct approach using fewer components. The LTC3706 controller is used on the secondary and the LTC3725 driver with self-starting capability is used on the primary. When an input voltage is applied, the LTC3725 begins a controlled soft-start of the output voltage. As the output voltage begins to rise, the LTC3706 secondary controller is quickly powered up via T1, D1 and Q2. The LTC3706 then assumes control of the output voltage by sending encoded PWM gate pulses to the LTC3725 primary driver via signal transformer, T2. The LTC3725 then operates as a simple driver receiving both input signals and bias power through T2.

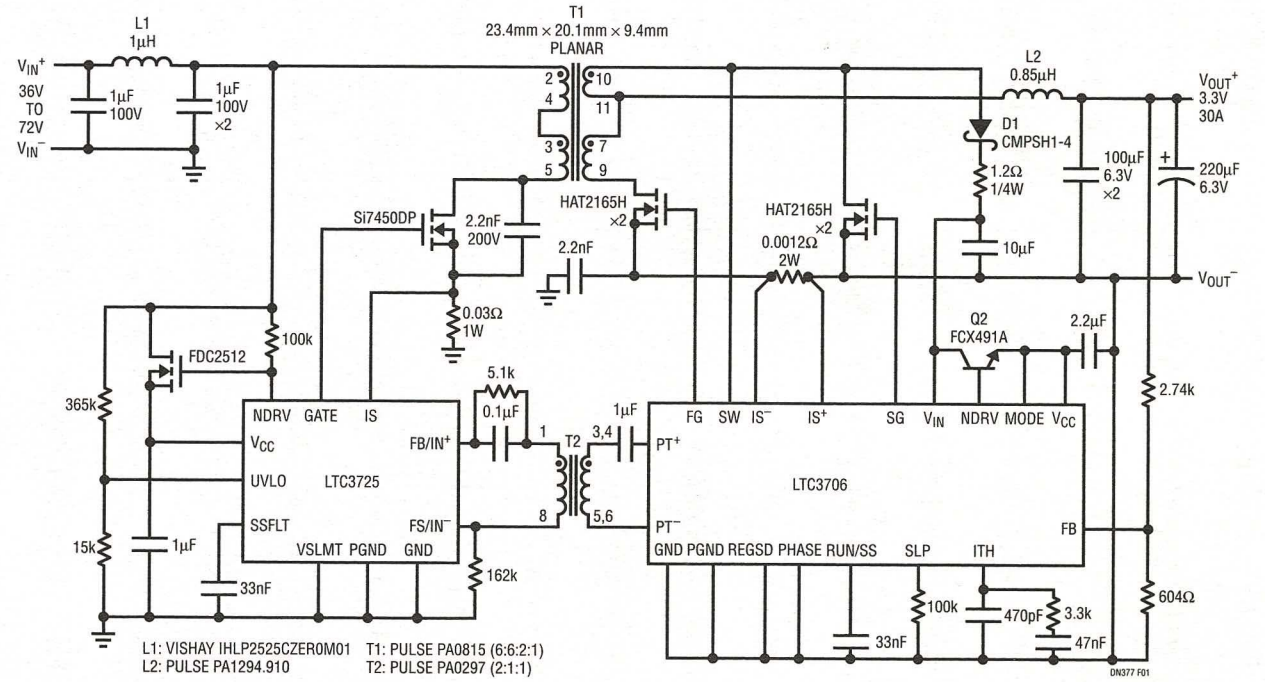

Figure 1. Complete 100W High Efficiency, Low Cost, Minimum Part Count Isolated Telecom Converter. Other Output Voltages and Power Levels Require Only Simple Component Changes

The transition from primary to secondary control occurs seamlessly at a fraction of the output voltage. From that point on, operation and design simplifies to that of a simple buck converter. Secondary sensing eliminates delays, tames large-signal overshoot and reduces output capacitance. The design shown in Figure 1 features off-the-shelf magnetics and high efficiency (see Figure 2).

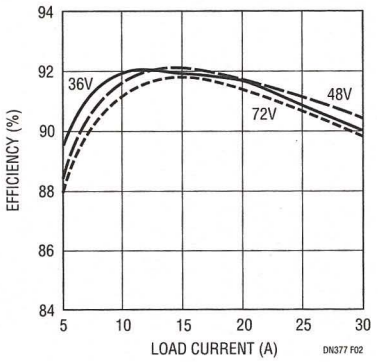

Figure 2. 36V to 72V_{IN} to 3.3V_{OUT} Efficiency

PolyPhase Design Ups Power Limit

The LTC3706 defies typical forward converter power limits by allowing simple implementation of a PolyPhase current share design. PolyPhase operation allows two or more phase-interleaved power stages to accurately share the load. The advantages of PolyPhase current sharing are numerous, including much improved efficiency, faster transient response and reduced input and output ripple.

The LTC3706 supports standard output voltages such a 5V, 12V, 28V and 52V as well as low voltages down to 0.6V. Figure 3 shows how easy it is to parallel two 1.2V supplies to achieve a 100A supply. Figure 4 shows the excellent output inductor current tracking during a 0A to 100A load current step and the smooth handoff during start-up to secondary-side control at 0.5V output.

Related Products

The LTC3705 is a dual switch forward driver version of the LTC3725 single switch forward driver. The LTC3705 includes an 80V (100V transient) high-side gate driver. The 2-switch topology eliminates transformer reset concerns, further simplifying design.

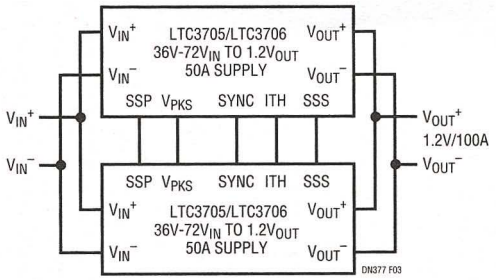

Figure 3. Paralleling Supplies for Higher Power Operation

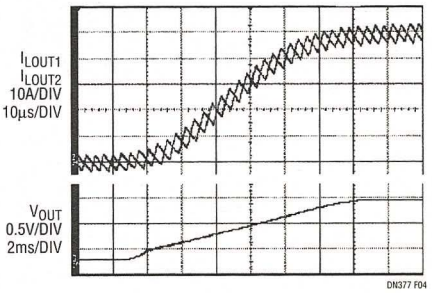

Figure 4. 1.2V, 100A Load Current Step (Top Trace) and Start-Up (Bottom Trace)

The 16-pin LTC3726 secondary controller is an option to the 24-pin LTC3706. The LTC3726 does not include the remote voltage sensing or the linear regulator features found in the LTC3706, so it is suitable in a single phase design or as a PolyPhase slave device. Both controllers may be used without the primary driver for nonisolated applications.

Features

These ICs include features that provide robust performance with few external parts and a simple feedback loop. For example, the LTC3725 primary driver includes a linear regulator controller and internal rectifier, eliminating the need for a primary bias supply. The LTC3725 also includes a volt-second and primary current limit. The LTC3706 controller includes a synchronous rectifier crowbar and remote voltage sensing.

Conclusion

The new LTC3706 controller and LTC3725 driver bring an unprecedented level of simplicity and performance to the design of isolated supplies. These two devices work together to offer high efficiency, low cost solutions using off-the-shelf external components.

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READERS SOLVE DESIGN PROBLEMS

Low-cost BER tester measures errors in low-data-rate applications

Cedric Mélange, Johan Bauwelinck, Jo Pletinckx, and Jan Vandewege,
Ghent University, Ghent, Belgium

You don't need an expensive pattern generator to produce a PRBS (pseudorandom-bit-sequence) signal for making elementary BER (bit-error-rate) measurements in low-data-rate continuous-transmission systems (**Reference 1**). You also need not spend time programming on a computer to compare sent and received data patterns. Moreover, most professional BER-measurement equipment doesn't cover lower bit rates. This Design Idea offers a simple, low-cost alternative that can accommodate data rates as high as 20 kbps. The system tests a 10-kbps transceiver in low-power sensor networks. The pattern generator, a Hewlett-Packard (www.hp.com) E1401B, can produce PRBS streams of only 150 kbps and higher.

An Atmel (www.atmel.com) AVR microcontroller creates a PRBS signal and compares the generated output stream with received data bits (**Figure 1**). After sending 1 million bits, the system displays the number of badly received bits on a two-row-by-16-character LCD. You can program the unit to transmit longer sequences of bits; however, doing so significantly increases the measurement time. Many low-cost or free development tools are available for AVR microcontrollers. This Design Idea uses an assembler and a serial programmer (**references 2** and **3**).

The design uses an 8-bit Fibonacci-type LFSR (linear-feedback-shift register) to produce the PRBS stream. The basic design includes a serial-shift register with modulo-2 addition using XOR instructions (**Figure 2**). You select the feedback taps' position to obtain a maximal-length sequence that has a period of 2^8-1 bits. Additional LFSR designs of different lengths and optimal feedback taps are also available (**Reference 4**). You can easily adapt the software in **Listing 1**, which is available for downloading at www.edn.com/

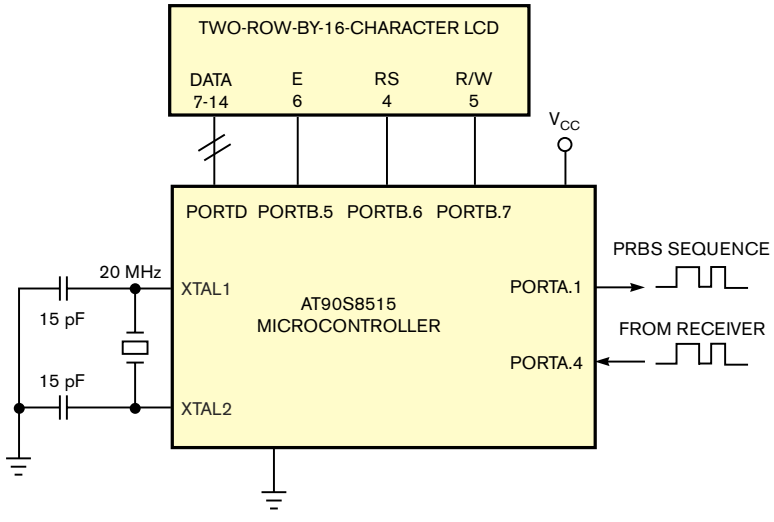

Figure 1 You can assemble a bit-error-rate-measurement circuit from only a few components.

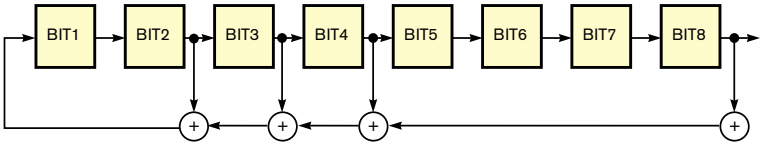

Figure 2 A linear-feedback-shift register generates a pseudorandom bit sequence.

DIs Inside

124 DMA eases CPU's workload for waveform generation

128 Bipolar current source maintains high output impedance at high frequencies

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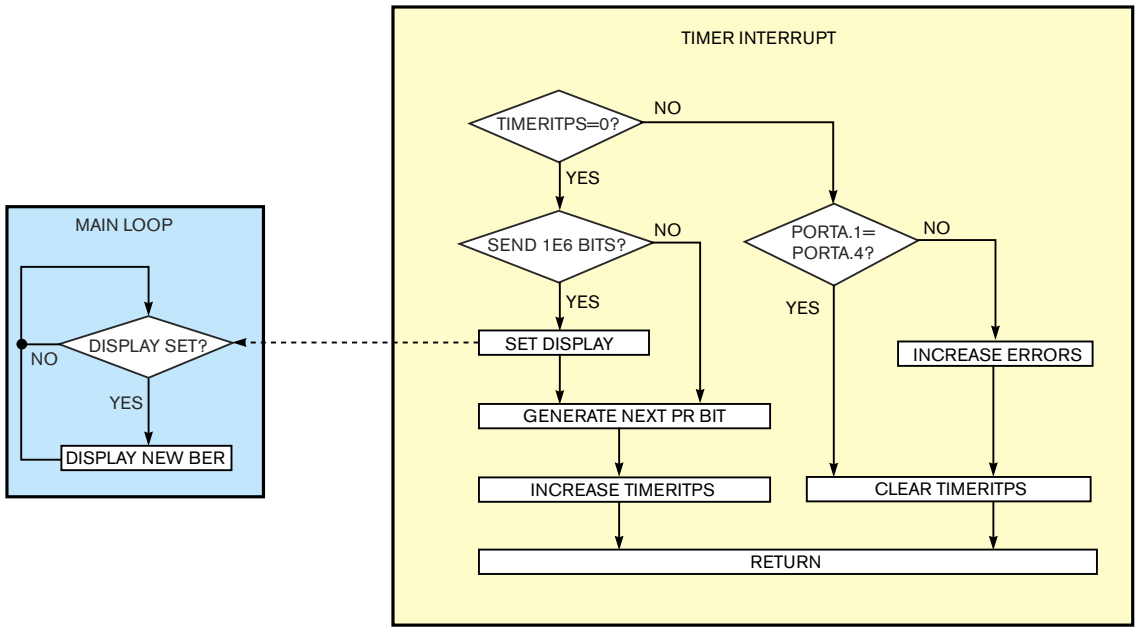

Figure 3 A simplified flow chart illustrates a BER tester's program subroutines.

051205di1 to produce PRBS signals with longer periods. A simplified flow chart of the assembler program is written for the AVR microcontroller (**Figure 3**).

The generated bit sequence appears at Pin Port A1, which you connect to a transmitter that's suitable for the system under test. Connect the digital output of a convenient receiver to Pin Port A4. The processor compares the received input with the output at Port A1 between two "send" bits. When the bits sent and received don't match, the number of displayed errors increases. If the system exhibits throughput delay, you need to modify the software to cope with the delay. EDN

REFERENCES

1 http://intec.ugent.be/design/.
2 AVRStudio 4, www.atmel.com.
3 SP12, www.xs4all.nl/~sbolt/e-spider_prog.html.
4 www.newwaveinstruments.com/resources/articles/m_sequence_linear_feedback_shift_register_lfsr.htm.

DMA eases CPU's workload for waveform generation

Mike Mitchell, Texas Instruments, Houston, TX

To generate analog voltages and waveforms, embedded systems often require one or more embedded or external DACs. To produce an analog voltage, the CPU must write the desired output value to the DAC at the appropriate time, a task that a timer-generated interrupt applied to the CPU usually initiates. In applications in which the DAC generates a periodic waveform, the CPU reads the next value from the table, sends it to the DAC, increments a table pointer, and checks for table boundaries to determine when to reset the table pointer.

Writing the periodic values to the DAC to maintain the output waveform requires CPU overhead, which varies depending on the data table's length, the output waveform's frequency, and the CPU's operating frequency. For example, using 32 data points per period to generate a 1-kHz sine wave requires the CPU to service 32,000 interrupts/sec. If the application requires a second analog output waveform, the CPU's loading increases, and updating both DACs within the required interrupt-service time may be impossible.

To calculate CPU loading, you need to know the length and the context-switching overhead of the ISR (interrupt-service routine). For the MSP430 processor, the ISR's overhead consumes 11 cycles, but the ISR's length depends upon how it is written. The assembly code in **Listing 1**, available at the Web version of this Design Idea at www.edn.com/051205di2, uses the fewest cycles to implement periodic waveform generation using one or two DACs. For a typical 1-MHz MSP430 CPU-instruction rate, serving 32,000 interrupts/sec leaves 1 million/32,000=

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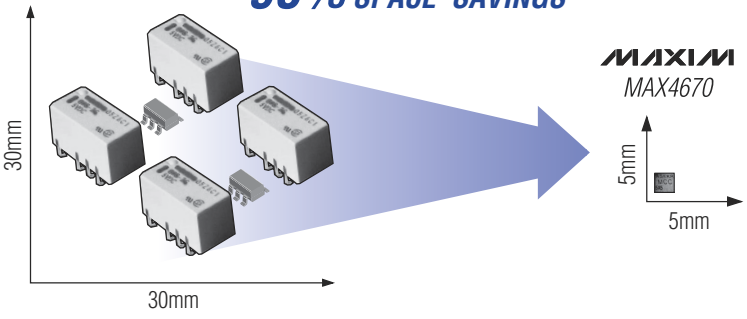

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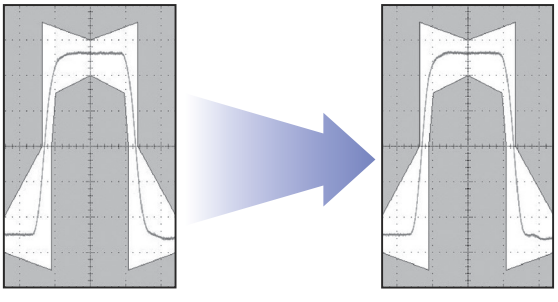

ACTUAL E1 TEMPLATE (NO REDUNDANCY)

ACTUAL E1 TEMPLATE USING MAX4670 PROTECTION SWITCH (8:1 REDUNDANCY)

Part	Configuration	Supply Voltage (V)	Tx R_{ON} (Ω)	Tx C_{ON} (pF)	Rx R_{ON} (Ω)	Rx C_{ON} (pF)	Surge Protection*	Package (mm x mm)
MAX4670	Octal SPDT	3.3	1.0	30	10	7	Yes	28-QFN (5 x 5)

*Surge protection meets GR-1089 intra-building, 2/10µs surge and IEC 61000-4-5, 8/20µs surge specifications (LIU-side protection).

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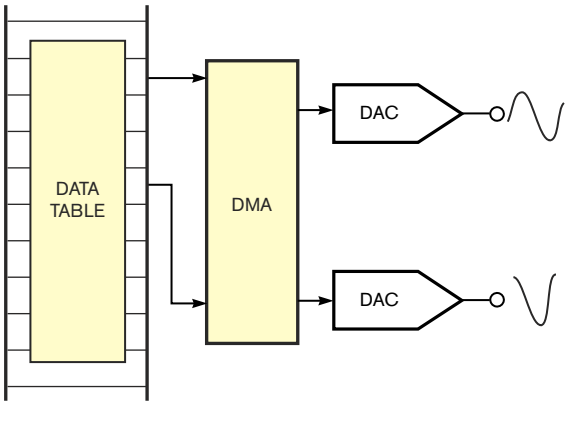

Figure 1 Using DMA, tabulated data values on their way to waveform-generating DACs avoid handling by a system's processor.

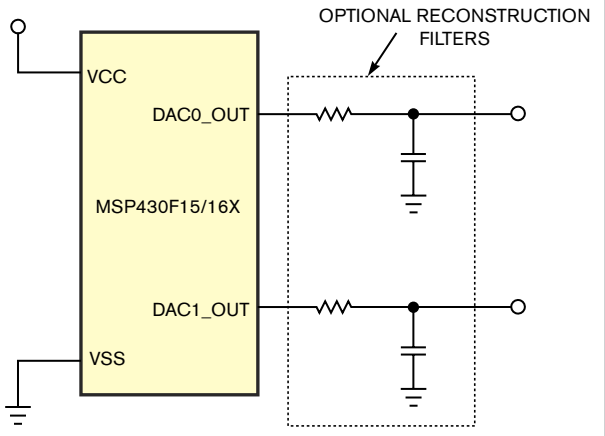

Figure 2 Optional lowpass filters on the DACs' outputs remove switching artifacts from the sine and the cosine waveforms.

31.25 CPU-instruction cycles between interrupts. An ISR requiring 18 cycles—that is, 18/31.25=57.6—represents a 57.6% CPU load. Supporting two DACs requires 23 cycles—that is, 23/31.25=73.6—and imposes a 73.6% CPU load. Increasing the MSP430's clock rate to its maximum 8 MHz reduces the CPU loading to 7.2 and 9.2%, respectively.

The required CPU load imposes limits not only on other tasks that the application may demand, but also on the waveform's maximum frequency. For example, a CPU operating at 100% CPU loading and an instruction rate of 1 MHz can generate a single waveform with a maximum frequency of approximately 1.73 kHz or two waveforms with a maximum frequency of approximately 1.35 kHz each. Raising the instruction rate to 8 MHz increases the respective maximum frequencies to approximately 13.9 and 10.9 kHz.

However, the MSP430F15x/16x family of devices includes a multichannel-DMA controller that can move data from one location to another without CPU intervention (**Figure 1**). In a waveform-generation application, the DMA controller moves data from the data table to the two DACs, significantly reducing the necessary CPU overhead to produce the waveforms. You can configure each of the DMA controller's three separate and independent channels to move a value from any address to any other address. In this example, one data table contains values for both the sine and the cosine waves, and two of the DMA channels simply access different parts of the table to form the sine and the cosine outputs. In addition, each DMA channel can independently increment its source or destination address. For this application, each DMA channel increments its source address, but the destination addresses of the respective DAC data registers always remain the same.

You can reconfigure each controller's preset number of DMA transfers. When either DMA channel has transferred its programmed number of data values, it begins the next data transfer from its originally programmed source address. In effect, each DMA channel treats its portion of the data table as a circular buffer to gener-

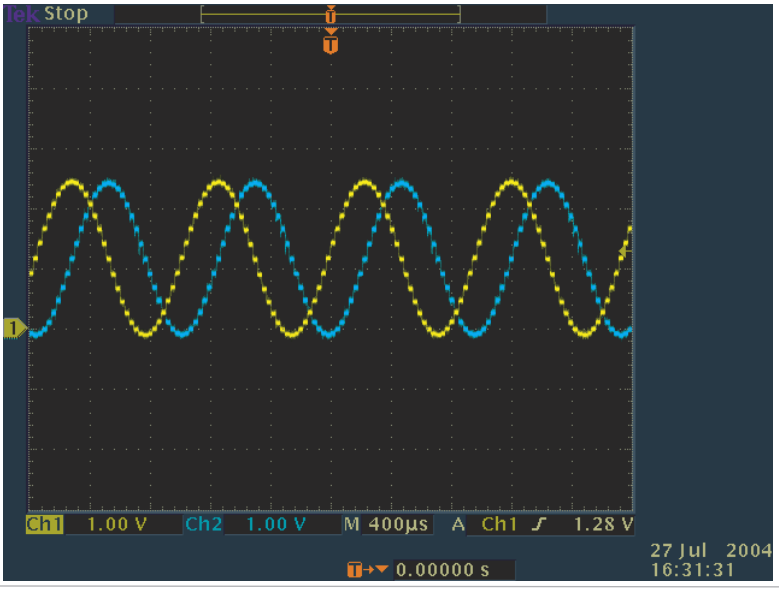

Figure 3 A phase shift occurs between the sine and the cosine output waveforms; removing the lowpass filters in Figure 2 reveals switching artifacts.

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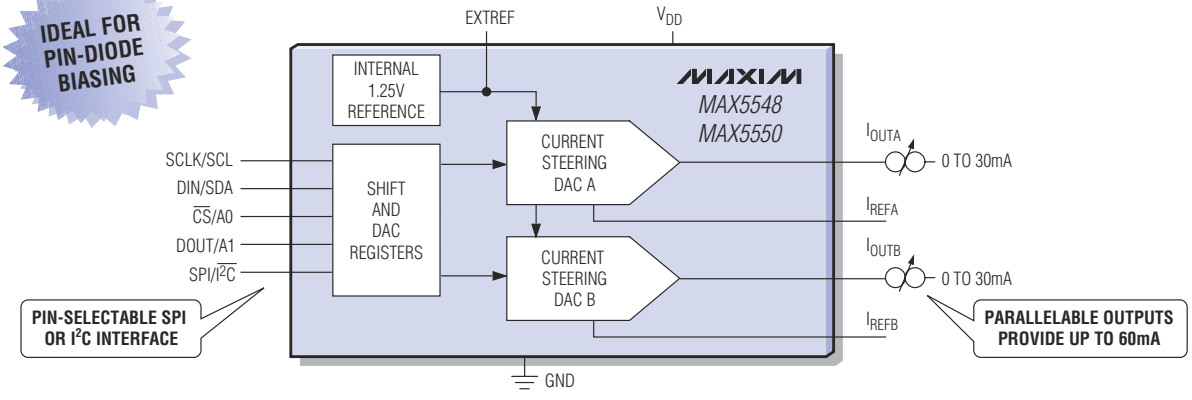

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MAX5550	10	-40 to +85	16-TQFN	3.37

16-TQFN ■ 3mm x 3mm

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ate a periodic waveform. Although DMA transfers do not involve the CPU, each transfer does consume two CPU clock cycles, which delays CPU code execution and thus introduces overhead. For the single-waveform example, using DMA transfers consumes two clock cycles for each DAC update instead of the 18 cycles necessary when using only the CPU. Thus, for a CPU clock rate of 1 MHz, using DMA reduces the effective CPU loading from 57.6% to 6.4% and increases the possible maximum output frequency from approximately 1.73 kHz to approximately 15.6 kHz. For an 8-MHz clock rate, using DMA reduces single-waveform CPU loading from 7.2% to 0.8%.

Generating two waveforms requires two DMA transfers or four clock cycles. For the two-waveform example, DMA reduces loading from 73.6% to 12.8% for a 1-MHz instruction rate, and from 9.2% to 1.6% for an 8-MHz rate. For the 1-MHz instruction rate, using DMA increases the possible maximum frequency for two waveforms from approximately 1.35 kHz to approximately 7.8 kHz.

After initialization, each DMA controller simply performs its duties with no further intervention other than receiving a trigger to move the data value. In this example, each DAC's interrupt flag serves as a trigger for its respective DMA channel. When you use dual DACs, you can load each DAC with the next value of waveshape data before it's required and then simultaneously trigger both DACs using a timer to avoid introducing delays that manifest themselves as output harmonic distortion. **Listing 2**, also available at www.edn.com/051205di2, contains software that generates sine and cosine waves and illustrates the DMA channels' independent operation apart from the CPU. Note that, after initialization of DMA channels and other device-specific peripherals, no further CPU activity occurs.

Figure 2 shows a partial schematic of the DACs' outputs. Depending on the application, you may need to add optional resistance-capacitance lowpass filters at the DACs' outputs. Select values for the resistor and capacitor in each filter to produce a pole in the filter response at the desired output frequencies. Note that the oscilloscope photo in **Figure 3** was taken with filters removed to show the DAC outputs' unfiltered waveforms. EDN

Bipolar current source maintains high output impedance at high frequencies

Alex Birkett, University College London, Hospital National Health Service, London, UK

Traditional current sources and voltage-to-current converters based on instrumentation and operational amplifiers offer high output impedances at low frequencies because of the amplifiers' good low-frequency CMRR (common-mode-rejection ratios). At higher frequencies, decreasing CMRR, inherent output capacitances, and slew-rate limitations prevent realization of high-quality current sources. Two 200-MHz line-receiver/amplifier ICs from Analog Devices, the AD8129 and AD8130, offer differential inputs and outstanding CMRR, making them strong candidates for building high-frequency constant-current sources. Al-

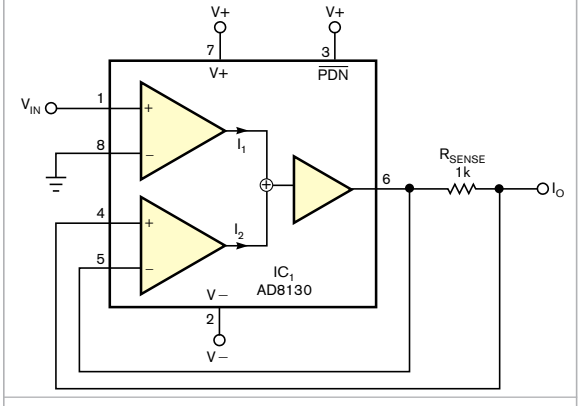

Figure 1 The 200-MHz AD8130 differential-input line receiver/amplifier can serve as a basic building block in a high-frequency-capable current source.

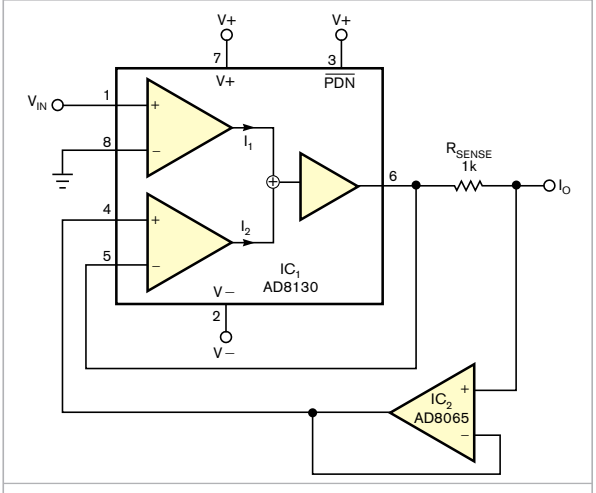

Figure 2 Adding an Analog Devices AD8065 buffer amplifier, IC_2, isolates the current-sampling resistor R_{SENSE} and reduces errors that IC_1's input-bias current contributes.

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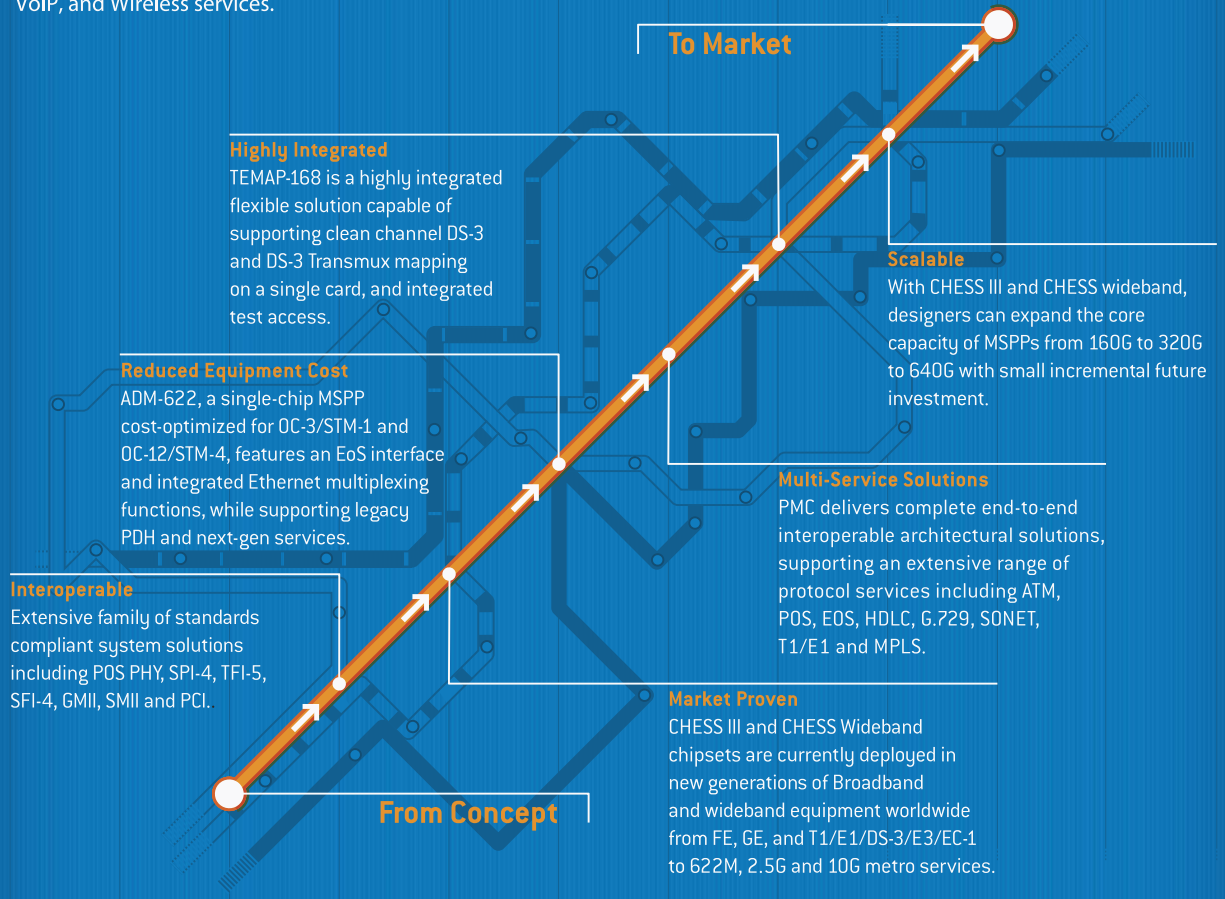

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though the circuit in **Figure 1** provides a good starting point, the AD8130's relatively high input bias current can affect output-current accuracy at low current levels.

To overcome the problem, you can add a unity-gain buffer, IC_2, to isolate the current-sense resistor (**Figure 2**). In addition, you can use the buffer amplifier to measure the load voltage and bootstrap the output cable's capacitance. The circuit presents an output impedance of about 500 kΩ at 1 MHz and a current-compliance range of 0 to ±3V using ±5V power supplies.

Current sources that have capacitance-coupled loads benefit from a dc servo loop to stabilize the circuit's operating point (**Figure 3**). The value of output-coupling capacitor C_O depends on the desired low-frequency roll-off characteristic. Further improvements of the basic circuit enable compensation of output capacitance and increase the circuit's output impedance. A small, adjustable feedback capacitor, C_{COMP}, that's approximately one-half of the output's stray capacitances provides feedforward compensation and further reduces the effects of stray capacitance at the output (**Figure 4**). To prevent oscillation, the cable's shield-driver circuit's gain should be slightly less than unity. Note that reducing the output-current-sense resistor, R_9, to 100Ω compensates for the input attenuator formed by R_1 and R_2 and maintains a 1-mA/V characteristic. This voltage-to-current source's frequency range spans 20 Hz to 10 MHz. For best results, use high-frequency circuit-layout and power-supply-bypassing methods. EDN

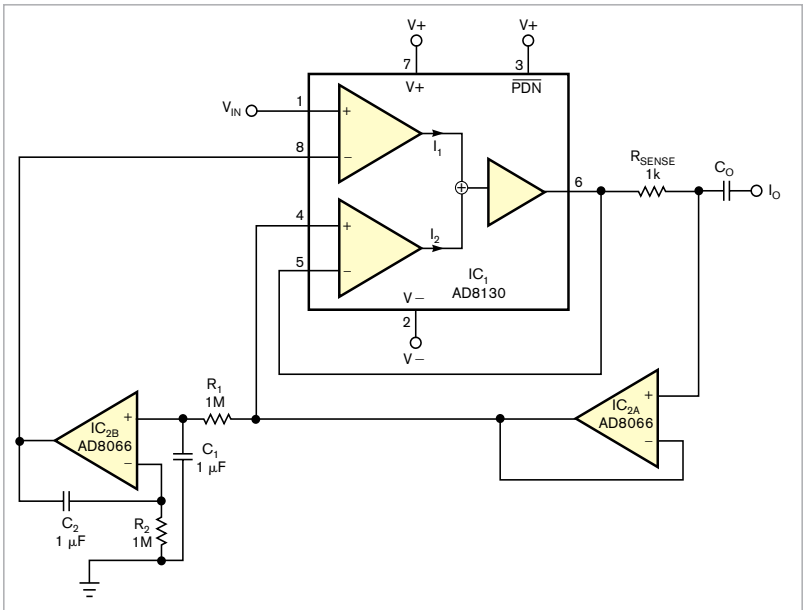

Figure 3 For an ac-coupled current output, add a dc-stabilization loop, IC_{2A} and IC_{2B}.

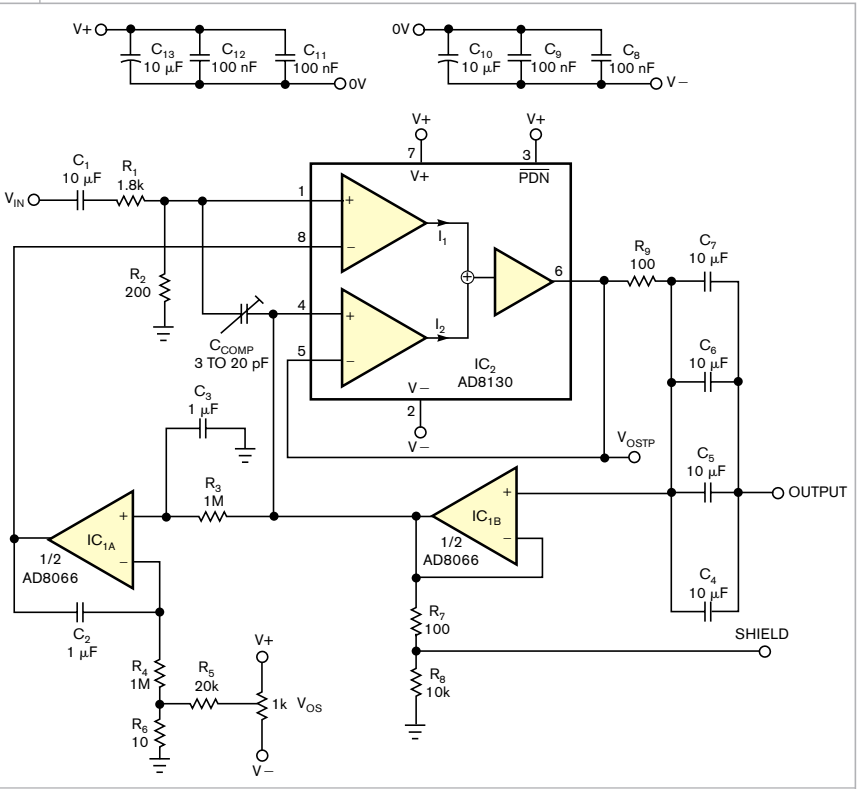

Figure 4 The complete circuit includes trimmer capacitor C_{COMP}, which compensates for stray capacitances in the circuit's packaged layout. Also, note wideband treatment of power-supply bypass capacitors.

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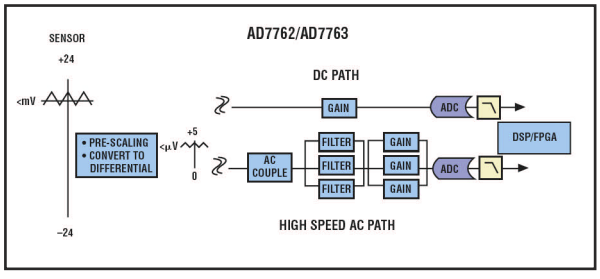
Currents Quarterly

Your First Look at New Analog and Mixed Signal ICs from Analog Devices

Fall/Winter 2005

AD7760/AD7762/AD7763—New High Speed 24-Bit ADCs Improve Accuracy While Simplifying Front End Signal Conditioning

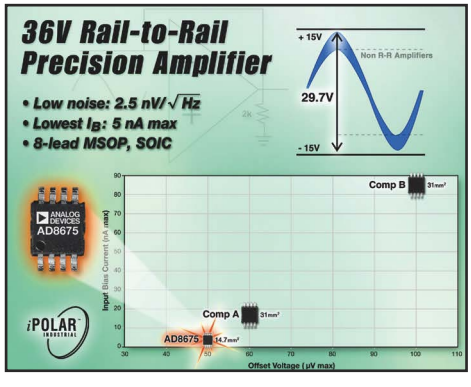


AD7760	$34.95
AD7762	$17.95
AD7763	$17.95

www.analog.com/AD7760
www.analog.com/AD7762
www.analog.com/AD7763

For those industrial and instrumentation applications that demand both high speed ac and accurate dc performance, Analog Devices now offers a new family of 24-bit converters that makes the benefits of Σ-Δ conversion available at much higher speeds. A wide dynamic range, combined with significantly reduced antialias filtering requirements, truly simplifies the design process and provides cost savings when compared to lower performance devices that require considerable front end signal processing. An integrated buffer to drive the reference, differential amplifier for signal buffering or level shifting, an overrange flag, programmable internal gain and offset registers, and a low-pass digital FIR filter make these devices compact, highly integrated data acquisition solutions for both ac and dc signals requiring minimal peripheral component selection. In addition, programmable decimation rates and ability to adjust the filter characteristics if the default characteristics are not appropriate significantly simplify high performance data acquisition, making the AD7760, AD7762, and AD7763 ideal for applications demanding industry-leading SNR without necessitating design of complex front end signal processing. The AD7760/AD7762/AD7763 are available in TQFP-64 packages.

36 V, Low Noise, Precision, Rail-to-Rail Output Op Amp



AD8675	$1.17

www.analog.com/AD8675

The AD8675 is a versatile, high precision op amp that combines low noise with an increased dynamic performance range. Enabled by ADI's *i*Polar trench isolation manufacturing process technology, the dual-supply AD8675 is only half the cost of competing amplifiers while reducing power 30%, lowering input bias current 75%, and providing 65% less drift over temperature. The new device also achieves three times the bandwidth and ships in a 3 mm × 5 mm, 8-lead MSOP (mini small outline plastic) package, just half the size of other amplifiers designed for high voltage industrial applications.

The AD8675 offers 2.5 nV/$\sqrt{\text{Hz}}$ noise, 2 nA max bias current, 2.5 mA supply current, and rail-to-rail output in an MSOP package. It is well-suited for applications where both ac and dc error sources cannot be tolerated. For applications with even lower error tolerances, the AD8675 has a proprietary offset nulling capability that allows a combination of both device and system offset errors up to 1 mV to be compensated externally. Unlike previous nulling schemes, the new technique does not degrade CMRR or offset drift performance of the amplifier.

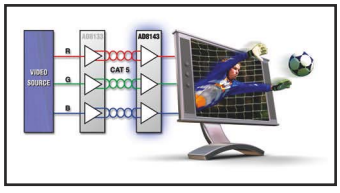
Highly Integrated ADL5350 Delivers Flexibility in Frequency Planning, Low Power Consumption, and Small Footprint for Wireless Applications

ADL5350 $2.35
www.analog.com/ADL5350

The ADL5350 is an RF (radio frequency) mixer that offers industry-leading linearity over a broad frequency range up to 3 GHz for both upconversion and downconversion applications. By delivering high linearity, very low power consumption, and high integration in a miniature 3 mm × 2 mm package, ADI's ADL5350 RF mixer reduces board space and cost while enabling designers to achieve no-compromise levels of performance. The ADL5350 excels in providing outstanding linearity for demanding applications such as GSM, CDMA, and WCDMA cellular base stations on a power budget, and the package footprint and price required by low cost portable applications, such as cellular phones.

The ADL5350 is the first single chip device to offer this combination of high linearity and exceptionally low power; it operates from a 3 V to 5 V supply and consumes only 16 mA of supply current. The device is packaged in a small 3 mm × 2 mm LFCSP (lead frame chip scale package), making it suitable for portable applications.

Triple Differential Receiver Simplifies Reception of Video Signals

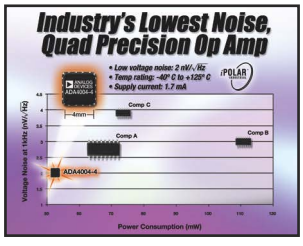


AD8143 $2.55
www.analog.com/AD8143

The AD8143 is a triple, low cost differential to single-ended receiver specifically designed for receiving RGB video signals over twisted pair cable. With a high common-mode rejection ratio (CMRR) of 70 dB at 10 MHz, the AD8143 eliminates the effects of induced electromagnetic interference (EMI) over long cables, further reducing cost by allowing for the use of unshielded twisted pair (UTP) cable. The AD8143 converts differential inputs to single-ended outputs, and the wide common-mode input range of ±10 V maintains signal integrity in systems where ground potential is different between the drive and receive ends. In addition to the three differential receivers, the AD8143 includes two auxiliary comparators, which can be used to receive digital signals from the fourth twisted pair of the Cat-5 cable, such as keyboard or mouse functions in KVM applications.

Package: 5 mm × 5 mm, 32-lead LFCSP

Lowest Noise, Precision, Quad Op Amp at 36 V

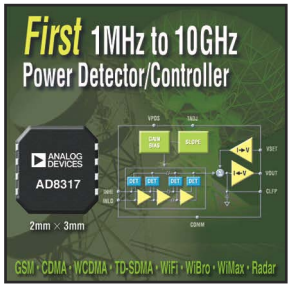


ADA4004-4 $3.02
www.analog.com/ADA4004-4

The ADA4004-4 offers industry-leading 2 nV/√Hz noise performance at just 1.7 mA/amp of supply current. This combination allows the best dynamic range over the extended industrial temperature range without incurring additional cooling or power penalties (e.g., fans, heat sinks). The LFCSP package saves board space, reduces cost, and improves layout flexibility. The ADA4004-4 is fully specified to operate from ±5 V to ±15 V over the extended temperature range –40°C to +125°C.

Packages: Pb-free, 4 mm × 4 mm, 16-lead LFCSP and 14-lead SOIC

Dual-Purpose Log Amp Accurately Measures and Controls RF Signals Over the Industry's Widest Frequency Range



AD8317 $3.93
www.analog.com/AD8317

The AD8317 is the industry's first RF (radio frequency) logarithmic detector/controller that accurately measures the power of radio signals from 1 MHz to 10 GHz, covering all cellular standards and a variety of wireless infrastructure and broadband wireless applications. In addition, the device offers fast output response time—enabling superior RF burst detection in radar applications—a tiny 2 mm × 3 mm package for space-constrained applications, and low power consumption for portable applications. These features, packed into one small IC (integrated circuit), allow manufacturers to reduce inventory and leverage design costs by having one device that can be used in several products.

The AD8317 provides precise, temperature-stable performance over the full range of –40°C to +85°C, as well as a very fast output response time of 5 nanoseconds, enabling RF burst detection beyond 125 MHz. The device operates over a supply voltage range of 3 V to 5 V, consuming only 20 mA of current; power consumption is reduced to less than 1 mW when the device is disabled.

AD1970—Complete MTS (BTSC) TV Stereo Encoder Delivers Enhanced Audio Experience

AD1970 $5.50
www.analog.com/AD1970

The AD1970 is an analog or digital in, analog out TV stereo digital audio processor with programmable MTS (BTSC) encoder that includes pilot-tone generation and subcarrier mixing functions. The stereo ADC provides the means for digitization of the analog baseband audio signal. A built-in high performance DAC is provided to output the BTSC baseband composite signal. The output of the AD1970 can be connected with minimal external circuitry to the input of a 4.5 MHz aural FM modulator.

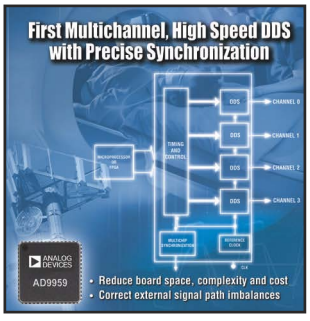
In addition to the digital BTSC encoder, the AD1970 includes a stereo image enhancement function, Phat Stereo™, to increase the sense of spaciousness available from closely spaced TV loudspeakers. A dialog enhancement algorithm solves the problem of playing wide dynamic range sources over limited-performance TV speakers and amplifiers. An I²C® port allows control of the AD1970's registers and parameters. The AD1970 is available in a 7 mm × 7 mm, 48-lead LQFP form factor.

ADV7180—Versatile NTSC/PAL/SECAM Video Decoder Enables Today's Advanced Video Formats

40-lead, 3-input LFCSP $5.64
64-lead, 6-input LQFP $5.92
www.analog.com/ADV7180

The ADV7180 automatically detects and converts standard analog baseband television signals compatible with worldwide NTSC, PAL, and SECAM standards into 4:2:2 component video data compatible with the 8-bit ITU-R BT.656 interface standard. The simple digital output interface connects gluelessly to a wide range of MPEG encoders, codecs, mobile video processors, and ADI's range of digital video encoders, such as the ADV7179. External HSYNC, VSYNC, and FIELD signals provide timing references for LCD controllers and other video ASICs, if required. 10-bit accurate A/D conversion provides professional quality video performance for consumer applications with true 8-bit data resolution. Three analog video input channels accept standard Composite, S-Video, or YPrPb video signals, supporting a wide range of consumer video sources. AGC and clamp restore circuitry allow an input video signal peak-to-peak range of 1 V. Alternatively, these can be bypassed for manual settings.

AD9959/AD9958—4-Channel/2-Channel, 500 MSPS DDS with Integrated 10-Bit DACs



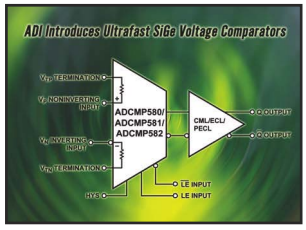
AD9958 $20.24
AD9959 $37.14
www.analog.com/AD9959

The AD9959 and AD9958 devices consist of four and two (respectively) independently programmable DDS channels. Since all channels share a common 500 MSPS system clock, they are inherently synchronized. If more than four channels are required, synchronizing multiple devices is a simple task. The AD9959 and AD9958 feature independent frequency, phase, and amplitude control of each channel; this allows for the correction of system channel imbalances due to analog processing such as filtering, amplification, or PCB layout related mismatches. The devices readily support frequency sweeping for radar and instrumentation applications. The devices incorporate an integrated high speed 10-bit DAC for each channel with excellent wideband and narrow-band SFDR. Each DDS has a 32-bit frequency tuning word, 14-bits of phase offset, a 10-bit output scale multiplier, and is available in a space-saving, 56-lead LFCSP package.

Applications

- Agile LO frequency synthesis
- Phased array radar/sonar
- Instrumentation
- Synchronized clocking
- RF source for AOTF

ADCMP580/ADCMP581/ADCMP582—The Newest Family of Ultrafast SiGe Voltage Comparators from ADI



ADCMP580	$7.00
ADCMP581	$7.00
ADCMP582	$7.00

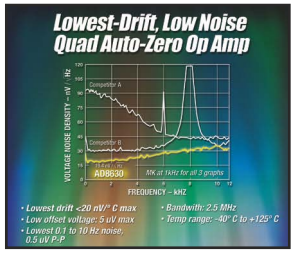
www.analog.com/comparators

Analog Devices continues to grow its already extensive portfolio of high speed and low power comparators with the release of the ADCMP580/ADCMP581/ADCMP582 ultrafast voltage comparators. The ADCMP580 features CML output drivers; the ADCMP581 features reduced-swing ECL (negative ECL) output drivers; and the ADCMP582 features reduced-swing PECL (positive ECL) output drivers.

These three comparators offer 150 ps propagation delay and 100 ps minimum pulse width for 10 Gbps operation with 200 fs random jitter (RJ). Overdrive and slew rate dispersion is typically less than 25 ps. The ±5 V power supplies enable a wide –2 V to +3 V input range with logic levels referenced to the CML/NECL/PECL outputs. The three inputs have 50 Ω on-chip termination resistors with the optional capability to be left open (on an individual pin basis) for applications requiring high impedance input.

High speed latch and programmable hysteresis are also provided. The differential latch input controls are also 50 Ω terminated to an independent VTT pin to interface to either CML or ECL or to PECL logic. The ADCMP580/ADCMP581/ADCMP582 are available in 16-lead LFCSP packages.

Zero-Drift, Low Noise, Rail-to-Rail Quad Op Amp for Precision Sensing Applications



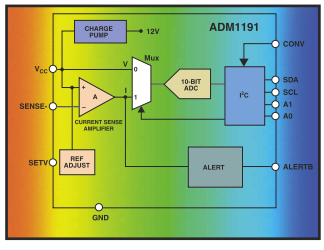
AD8630	$2.70

www.analog.com/AD8630

The AD8630 is designed for precision sensing applications where error sources cannot be tolerated. The AD8630 has the lowest noise (0.5 μV p-p, 0 Hz to 10 Hz) and lowest drift (less than 0.02 μV/°C max) of any auto-zero amp on the market today, and offers a low offset voltage of only 5 μV max. It operates on a single supply from 2.7 V to 5 V and has rail-to-rail input and output swing. The AD8630 is fully specified for operation over the extended industrial temperature range of –40°C to +125°C.

Packages: Pb-free, 14-lead TSSOP and SOIC surface mount

ADM1191/ADM1192—Digital Power Monitor with Convert Pin and Extended Addressing



ADM1191	$1.15
ADM1192	$1.15

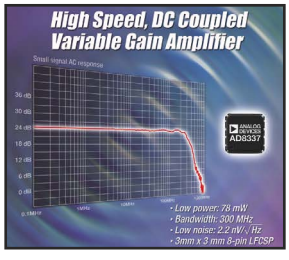
www.analog.com/ADM1191
www.analog.com/ADM1192

The ADM1191 offers digital current and voltage monitoring via an on-chip 10-bit ADC, communicated through an SMBus interface. An internal current sense amplifier senses voltage across the sense resistor in the power path via the VCC and SENSE pins. A 10-bit ADC is configured to be able to measure the current seen in the sense resistor and also the supply voltage on the VCC pin. The current sense amplifier.

An industry-standard SMBus interface allows a controller to read current and voltage data from the ADC. Measurements can be initiated by an SMBus command write or via the CONV pin. Alternatively, the ADC can run continuously and the user can read the latest conversion data whenever it is required. Up to 16 unique SMBus addresses can be created by the way the A0 and A1 pins are connected.

A digital overcurrent level can be programmed. The AlertB output flag will assert if this level is exceeded. Overcurrent events can be cleared via the SMBus. The ADM1191 is available in a 10-lead MSOP package.

Designs Using Low Cost, DC-Coupled VGA Boost Bandwidth and Cut Power Requirements



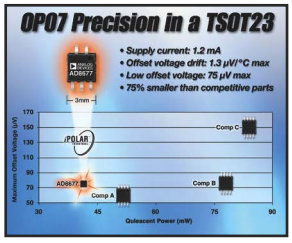
AD8337	$2.49

www.analog.com/AD8337

Designers of industrial and instrumentation equipment often need to balance good dc performance with high bandwidth and low power requirements. Trade-offs can affect the accuracy and consistency of the design. The AD8337 dc-coupled, single-ended variable gain amplifier (VGA) strikes a balance by offering up to 50% more bandwidth (300 MHz at –3 dB) and 25% lower power per channel than competitive devices. The AD8337 topology is an X-AMP® structure with 24 dB of gain range with excellent bandwidth uniformity across the entire gain range. The gain control interface provides precise linear-in-dB scaling of 20 dB/V and can be centered by an output common-mode adjust pin. The AD8337 offers low noise (2.2 nV/$\sqrt{\text{Hz}}$) and variable gain at frequencies up to 100 MHz.

Package: 3 mm × 3 mm, 8-lead LFCSP

Enhanced OP07 Performance in Tiny TSOT-23



The AD8677 addresses the need for system performance in a small footprint. The 5-lead TSOT-23 packaging is 75% smaller than the competition and improves layout flexibility by saving board space and costs. The AD8677 reduces power consumption by as much as 40% as compared to OP07 standard types. Higher CMRR and PSRR improve accuracy in noisy environments. With 80° phase margin, the AD8677 is stable for nearly any capacitive load in any configuration, despite PC board input parasitics. The AD8677 operates from ±5 V to ±15 V and is specified over the extended industrial temperature range (–40°C to +125°C).

Packages: Pb-free, 5-lead TSOT-23 and narrow, 8-lead SOIC

AD8677	$0.75

www.analog.com/AD8677

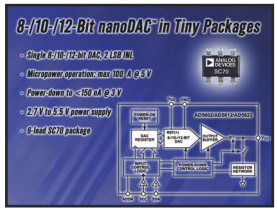
AD9736/AD9735/AD9734—14-/12-/10-Bit, 1.2 GSPS TxDAC+® D/A Converter Family

The AD9736, AD9735, and AD9734 are high performance, high frequency DACs that provide sample rates of up to 1,200 MSPS, permitting multicarrier generation up to their Nyquist frequency. The AD9736 is the 14-bit member of the family, while the AD9735 and the AD9734 are the 12-bit and 10-bit members, respectively. They include a serial port interface (SPI) that provides for programming many internal parameters and also enables readback of status registers. They use a reduced specification LVDS interface to minimize data interface that may degrade performance. The output current can be programmed over a range of 10 mA to 30 mA. The AD9736 family is manufactured on a 0.18 µm CMOS process and operates from 1.8 V and 3.3 V supplies for a total power consumption of 380 mW in bypass mode. The devices are supplied in a 160-ball BGA package for reduced package parasitics.

AD9736	$34.95
AD9735	$19.95
AD9734	$14.95

www.analog.com/AD9736

AD5602/AD5612/AD5622—*nano*DAC Family Extends Its Portfolio of 8-Bit to 12-Bit DACs in Tiny SC70 Packages



The AD5602/AD5612/AD5622, members of the *nano*DAC family, are single, 8-/10-/12-bit buffered voltage-output DACs that operate from a single 2.7 V to 5.5 V supply, consuming <100 µA at 5 V. These DACs come in tiny SC70 packages. Each DAC contains an on-chip precision output amplifier that allows rail-to-rail output swing to be achieved.

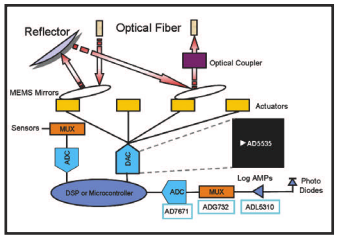
The AD5602/AD5612/AD5622 use a 2-wire, I²C-compatible serial interface that operates in standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes.

The references for AD5602/AD5612/AD5622 are derived from the power supply inputs to give the widest dynamic output range. Each part incorporates a power-on reset circuit that ensures the DAC output powers up to 0 V and remains there until a valid write takes place at the device. The parts contain a power-down feature that reduces the current consumption of the devices to <100 nA at 3 V and provides software-selectable output loads while in power-down mode. The parts are put into power-down mode over the serial interface. The low power consumption of the AD5602/AD5612/AD5622 in normal operation makes them ideally suited for use in portable battery-operated equipment. The typical power consumption is 0.4 mW at 5 V.

AD5602	$0.93
AD5612	$1.15
AD5622	$1.32

www.analog.com/nanoDAC

New 200 V, 32-Channel *dense*DAC™ in 15 mm × 15 mm Footprint



As part of the *dense*DAC family of high resolution and high channel count DACs, the new AD5535 achieves full-scale output voltage programmable from 50 V to 200 V, in industry-leading packaging. The user can select the output voltage range via a programmable REF_IN pin, e.g., the output range is 0 V to 50 V with REF_IN = 1 V and is 0 V to 200 V with REF_IN = 4 V. The AD5535 is guaranteed monotonic to 14 bits, and each output amplifier can source 700 µA, making it ideally suited for optical communication applications such as MEMS mirror control switches and attenuation level control (VOA).

The selected DAC register is written via the 3-wire SPI interface, which operates at clock rates up to 30 MHz. The AD5535 operates with AV_{CC} = 5 V, DV_{CC} = 3 V to 5 V, V– = –5 V, V+ = +5 V, and V p-p = 210 V. It is packaged in a 124-ball CSPBGA package with a footprint of 15 mm × 15 mm.

AD5535	$135.00

www.analog.com/AD5535

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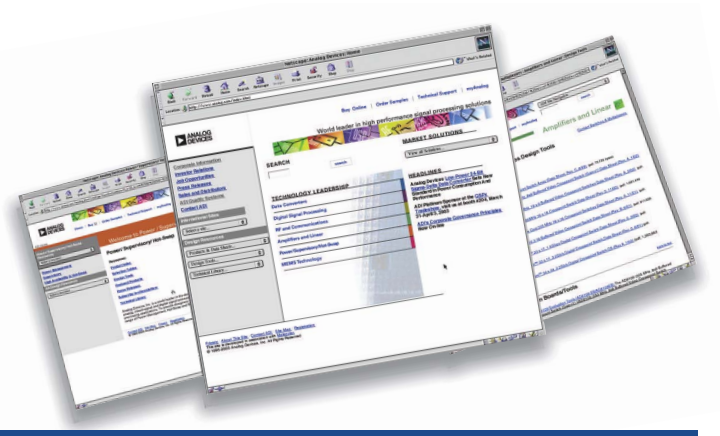
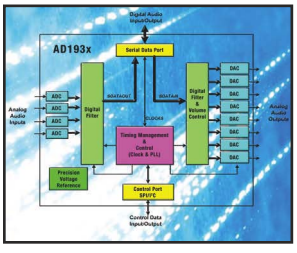


For a complete list of products released this quarter and to order samples, please go to *www.analog.com/currents*.

Converters — Family of 4 ADC/8 DAC, 192 kHz, 24-Bit Audio Codecs with PLL



AD193x	Contact ADI
www.analog.com/AD1935	
www.analog.com/AD1936	
www.analog.com/AD1937	
www.analog.com/AD1938	
www.analog.com/AD1939	

The AD193x family of high performance single-chip audio codecs provides four ADCs with differential input and eight DACs with either single-ended or differential output using ADI's patented multibit Σ-Δ architecture. An SPI® or I²C port is included, allowing a microcontroller to adjust volume and many other parameters. The AD193x family operates from 3.3 V digital and analog supplies. The AD193x is available in a 48-lead (SE output) or 64-lead (differential output) LQFP package.

The AD193x is designed for low EMI. This consideration is apparent in both the system and circuit design architectures. The AD193x eliminates the need for a separate high frequency master clock. It can also be used with a suppressed bit clock. The D/A and A/D converters are designed using the latest ADI continuous time architecture to further minimize EMI. By using 3.3 V supplies, power consumption is minimized, further reducing emissions.

Converters — ADT75—±2°C Accurate, 12-Bit Digital Temperature Sensor

ADT75	$0.65
www.analog.com/ADT75	

The ADT75 is a complete temperature monitoring system that consists of a band gap temperature sensor and a 12-bit ADC to monitor and digitize the temperature to a resolution of 0.0625°C. The ADT75 is pin and register compatible with the LM75 and AD7416 and the ADT75 is specified for operation at supply voltages from 3 V to 5.5 V. Operating at 3.3 V, the supply current is typically 300 μA. The ADT75 offers a shutdown mode that powers down the device and gives a shutdown current of typically 3 μA. The device is rated for operation over the –55°C to +125°C temperature range. The ADT75 is available in both an 8-lead MSOP and SOIC package.

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ANALOG DEVICES

www.analog.com/currents

productroundup

PASSIVES

Power-cube-inductor series provides wide OCL range

Targeting PC motherboard and server markets, the PG0322NL series aims at VRMs (voltage-regulated modules), dc/dc converters, and point-of-load applications. With an operating temperature of −40 to +130°C, the series also features a 32 to 60A heating-current rating and a 30 to 50A current-saturation capability, suiting high-current, multiphase buck-converter applications. Features include a 0.28- to 1.2-μH OCL (open-circuit inductance), allowing for a choice of inductance value for ripple current and system transient response and a 0.6- to 1.65-mΩ DCR (direct-current-resistance) range for higher system efficiency due to lower copper losses. Measuring 14.5×14.5×9.5 mm, the inductors comply with ROHS (reduction-of-hazardous-substances) guidelines and the EIA481 standard. The PG0322NL series costs 18 cents (100,000).

Pulse, www.pulseeng.com

Compact 1206 chip inductors offer 1A-class power rating

With a maximum height of 0.9 mm, the CKP3216 series of 1206-case multilayer-chip inductors suits use in dc/dc-converter choke coils. The series features current ratings of 0.7 to 1.1A and 4.7 to 1 μH. An internal-electrode printing press enables the vendor to double the thickness of the internal conductor, providing lower dc resistance than the vendor's previous-generation devices. The CKP3216 series costs 20 cents.

Taiyo Yuden Inc, www.yuden.us

Thermal gap filler targets telecom and computing applications

Targeting use in computer and telecommunication applications, the T-flex 300 thermally conductive gap fillers provide component and device performance integrity. Peripherals include

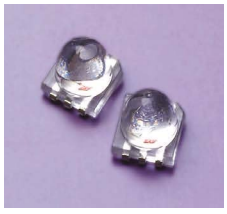
1.2W/mK thermal conductivity, an ultrasoft interface pad that conforms with minimal pressure, an optional metallized liner with a low-friction surface, and electrical insulation. Thickness ranges from 0.25 to 5.08 mm. The T-flex 300 targets notebook computers, mobile-telecommunication devices, and high-speed mass-storage.
Laird Technologies, www.lairdtech.com

Interconnect technology suits a range of applications

A Q-shaped contact provides the iQ interconnect connector with a low profile and a large working range. The 0.081 profile results in short signal paths with 0.6-nH self-inductance and 12-mΩ resistance, minimizing crosstalk. Features also include a low compression force, reducing stress on mating components; a 1-mm, high-density pinout; and floating contacts that shift to adjust for uneven planarities. The technology suits land-grid-array, flex-circuit, board-to-board, and component-to-board applications.
Cinch Connectors, www.cinch.com

Auxiliary LED flash enables autofocusing in low-light conditions

Providing illumination to operate the automatic-focus function of digital still cameras under low-light conditions at a range of 3m, the high-brightness ASMT-FJ10 LED features an 18-cd-at-20-mA light output. Instead of using infrared-emitting LEDs, this device uses visible light, allowing the use of the same autofocus sensor for low-light and ordinary conditions. An orange, 612-nm LED also provides visible illumination, allowing the use of the same device as a red-eye-reduction lamp and as an indicator for a camera's self-timer. Measuring 4.8×4.8 mm, the ASMT-FJ10 LED costs 35 cents.



Agilent Technologies Inc, www.agilent.com

Ferrite-drum-core inductors have wide-ranging inductance values

The SPB-700 series of ferrite-drum-core inductors comprises 26 parts with inductances of 180 µH at 15A to 22,000 µH at 2.7A dc. Measuring 53.3×37.08 mm, the device also has a mounting hole through the center of the core, accepting #6 through #10 nonmetallic screws. The two leads extend from the bottom of the core, 180° apart from each other. The SPB-700 series costs $12.
Prem Magnetics, www.premmagnetics.com

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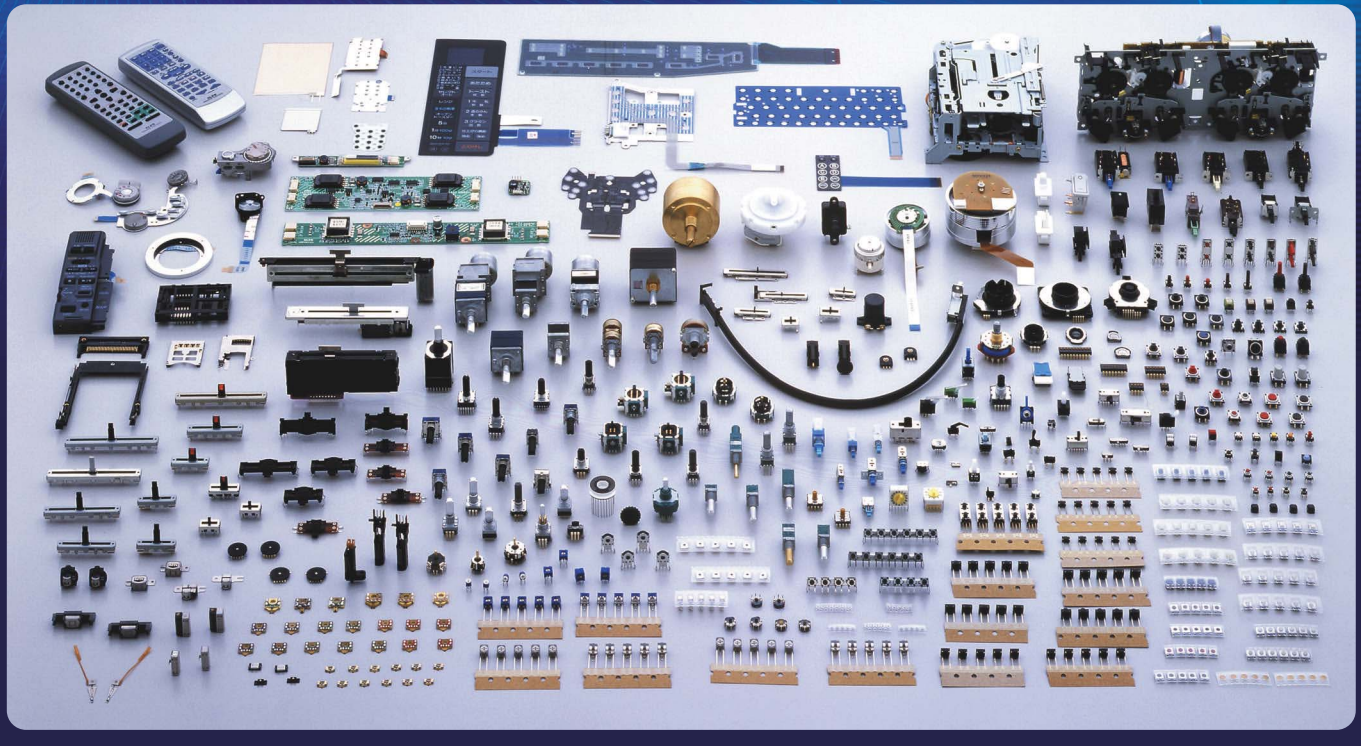

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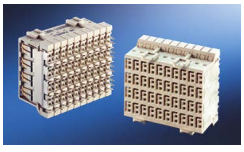
ZD connector series adds female vertical version

A new part in the high-speed ERmet ZD line, a four-row, vertical, female connector requires high-performance board-to-board connectors when expanding modern assembly systems, implementing mezzanine applications, or transferring signals through the rear I/O. With two, three, and four rows of contacts, the right-angle connector provides fast transmission of signals, high contact density, and support for PICMG 2.20, 3.0 (ACTA), or EXP.0. Including 40 differential-signal pairs, the connector currently has a 15-mm assembly height; the vendor plans 12- and 22-mm assembly heights.



ERNI, www.erni.com

Tantalum capacitor provides 3300-µF capacitance

As an alternative to multiple low-value capacitors for sufficient capacitance in low-profile applications, the Sprague 592D tantalum capacitor provides 3300 µF in a 2.5-mm-high package. This conformal-coated, solid-tantalum capacitor suits noise-suppression, filtering, coupling, and timing applications, such as PCMCIA cards, power supplies, line cards, and cell phones. The devices in the X case come in 4 to 6.3V ratings and in 1000-, 1500-, 2200-, and 3300-µF capacitances. A low maximum-ESR range includes 0.055Ω at 25°C and 100 kHz for the 3300-µF model.

Vishay Intertechnologies, www.vishay.com

COMPUTERS & PERIPHERALS

SOC supports perpendicular recording

Targeting use in miniature hard-disk drives, the SC1200 SOC (system on chip) supports perpendicular recording, CE-ATA, and MMC (multimedia-card) host-bus-interface options. The chip has a 0.5-dB performance advantage, a 10% capacity increase, and a 30% smaller die than the vendor's previous SOC design. For 1-in. disk drives, the device stores 12 Gbytes. The chip set operates at 350 Mbps and features 1.8 and 3.3V configurations for low-power operation. The SC1200 costs $10.

Agere, www.agere.com

Hard-drive series has four models

The P120 Series features 200- and 250-Gbyte parallel and SATA versions with 3-Gbps hard-disk drives. All

P120 hard drives include a 7200-rpm spindle speed, an 8.9-msec average seek time, and an 8-Mbyte cache buffer. Targeting demanding applications, the 200-Gbyte SP2004C costs $150, and the 250-Gbyte SP2504C costs $170. The 200-Gbyte SP2014N and 250-Gbyte SP2514N have Ultra ATA-133 interfaces and cost $130 and $150, respectively.

Samsung Electronics, www.samsung.com

Two-drive, 3-Gbps SATA processor eases RAID configurations

The 1-Tbyte, 3-Gbps, two-drive SiI 4723 SATA storage processor employs the vendor's Steelvine architecture, which enables designers to easily configure RAIDs (redundant arrays of inexpensive disks). The device also supports data mirroring for RAID 1 or safe mode, data stripping for RAID 0 or fast mode, drive spanning for concatenation or big mode, and JBOD (just a bunch of disks) for port-multiplier mode. Designers can achieve higher virtualization by connecting to a port-multiplier-aware SATA host controller. The SiI 4723 costs $15 (10,000).

Silicon Image Inc, www.siliconimage.com

4-Gbyte hard drive suits portable players, guards against damage

The Crash Guard II ruggedness feature protects the 4-Gbyte SE (storage element), which targets use in MP3 players, cell phones, GPS devices, and personal video recorders. Crash Guard II comprises an active latch, removing the head from the disk and locking it in place when a user drops the hard drive; skip control, providing continuous playback without skipping or restarting; and drop safe, which activates the active latch when a user drops the hard drive while it is reading or writing data to the disk. The device costs $65 (10,000).

Cornice Inc, www.corniceco.com

High-performance external hard drives have FireWire connectivity

Two nine-pin standard FireWire 800 connectors allow for an 800-Mbps transfer rate for the Rocpro 800 AV. Capacities include 120, 160, 200, 250, 300, and 400 Gbytes, all with a 7200-rpm rotation speed. Additional peripherals include a standard FireWire 800/IEEE 1394b interface, an Oxford 922 chip set, an 8.9-msec average seek time, and a 2.9-lb weight. A 5.8×8.7×1.6-in. footprint provides stackable and upright configuration options. The Rocpro 800 AV costs $129.

Rocstor, www.rocsecure.com

Stereo codec suits midlevel and entry-level digital-audio applications

Using a multibit delta-sigma architecture, the CS4270 provides an ADC and a DAC with 24-bit resolution at a 216-kHz audio-sampling rate. Single-ended inputs and outputs allow 95- to 105-dB total harmonic distortion plus noise. Able to operate on a 3.3 or 5V power supply, the codec features on-chip level shifters for logic levels of 1.8 to 5V, and it has Popguard technology for controlling power-cycling "clicks" and "pops." The CS4270 comes in a TSSOP-24 and costs $2.43 (10,000).

Cirrus Logic Inc, www.cirrus.com

Video processor has a variety of on-chip features

Running at 500 MHz, the BSP-16 video processor includes on-chip processors featuring a fast 2-D DMA engine, a RISC coprocessor, an on-chip video filter, and a 3DES engine for hardware encryption and decryption. The chip's additional features include BT.1120 high-definition-stream input processing; BT.6956 multiple standard-definition digital-video streams; four I^2S audio inputs; eight I^2S audio-stream outputs; an on-chip display-refresh controller; a glueless DDR-SDRAM controller; and on-chip Ethernet, IDE, and NAND flash controllers. With speeds of 350 to 500 MHz, the BSP-16 video processor costs $20.

Equator Technologies Inc, www.equator.com

CMOS image-sensor series adds a 3.2 million-pixel chip

As part of the Dynastron CMOS image-sensor line, the 3.2 million-pixel ET8E99-AS chip has a 2.7-micron pixel pitch with a 1/2.6-in. optical format and incorporates an ADC. Features include a 15-frame/sec frame rate at QXGA output and 30 frames/sec at 3-to-1, vertical-pixel binning, automatic blemish detection and correction, gain-control and lens-shading compensation, and a PLL circuit. The ET8E99-AS costs $45 (1000).

Toshiba America Electronic Components Inc, www.chips.toshiba.com

Six-channel DAC has fewer "clicks" and "pops"

A multibit delta-sigma architecture is the core of the CS4361's six-channel DAC. Features include a 105-dB dynamic range, low-latency digital filtering, automatic sample-rate detection, and on-chip level translators. The device also includes proprietary Popguard technology, which reduces the "clicks" and "pops" of power cycling. The CS4361 comes in a TSSOP-20 package and costs $2.70 (10,000).

Cirrus Logic Inc, www.cirrus.com

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realitycheck

YESTERDAY'S HYPE MEETS TODAY'S REALITY

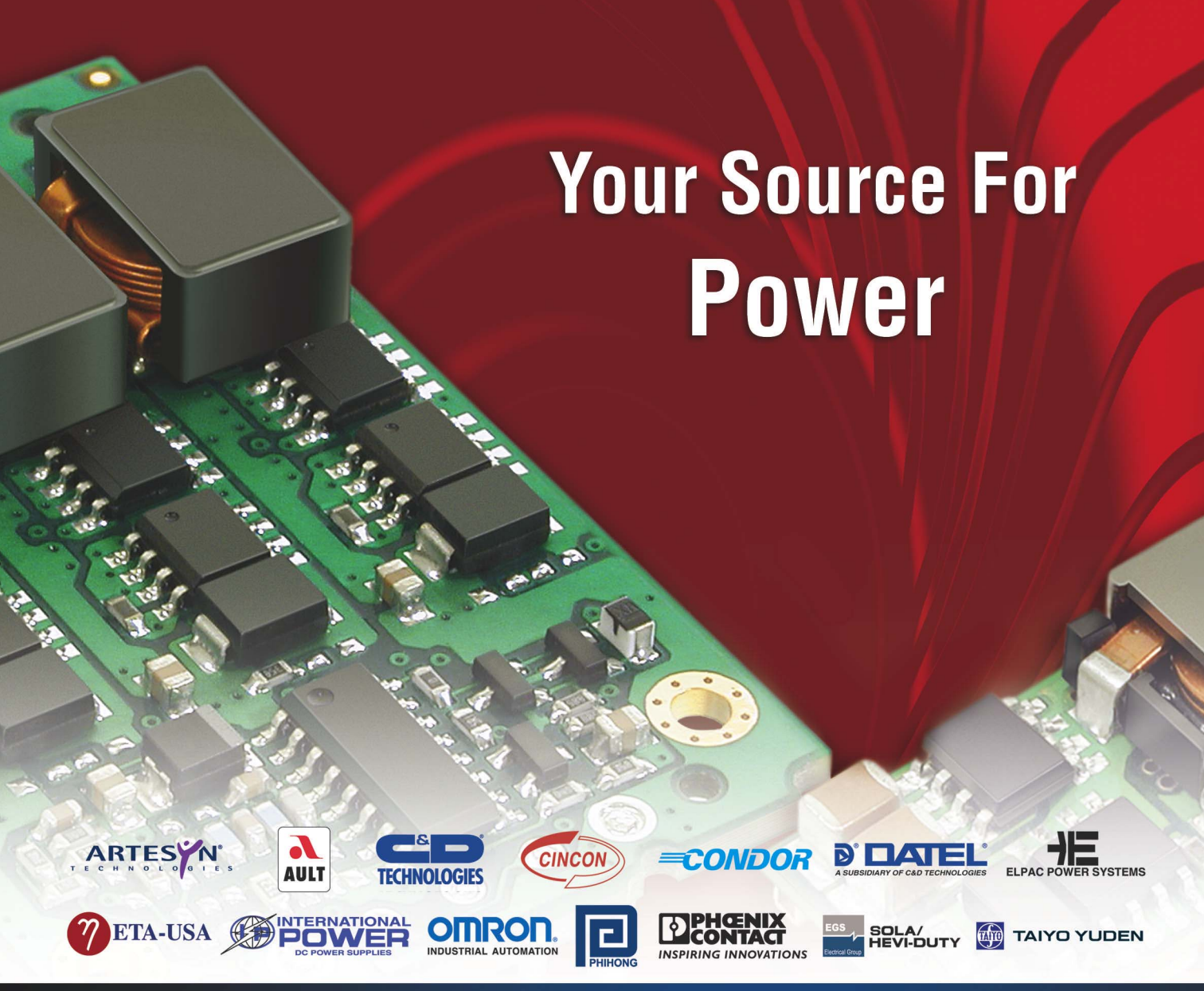
STATS Price: $395 / Weight: 8.7 oz / Manufactured from 1972 to 1975 / Number sold: 300,000

An abacus in your pocket

In 1972, market studies indicated that a pocket-sized scientific calculator would go nowhere, but that didn't deter Bill Hewlett and his company, Hewlett-Packard, from developing the Abacus HP-35 handheld calculator. Hewlett wanted to sell a pocket-sized version of its first electronic calculator, the 40-lb 9100A, which HP developed in 1968. The HP-35, as it turned out, was more precise than some mainframe computers. Within months of the calculator's introduction, GE (www.ge.com) ordered 20,000 units, according to The Museum of HP Calculators (www.hpmuseum.org). When someone discovered a bug after HP had shipped 25,000 units, the company offered free replacements.

The rest is history. HP scientific calculators are standard fare today—with everyone from high-school math students to seismologists. Electrical Engineer David Hicks founded the Museum of HP Calculators, which claims no affiliation with HP. Hicks is only one of many calculator collectors who worship the older HP, Sharp, and TI scientific calculators, some of which you can read about at the Datamath Calculator Museum (www.datamath.org/SciWEDGE/sr-50.htm). TI introduced the SR-50 electronic slide rule in 1973 at less than half the HP-35's price.

—by John Dodge



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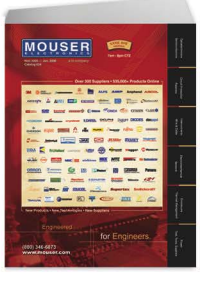

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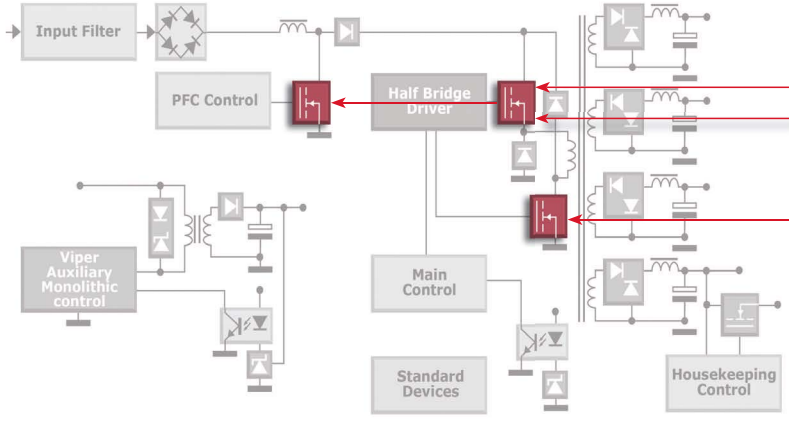

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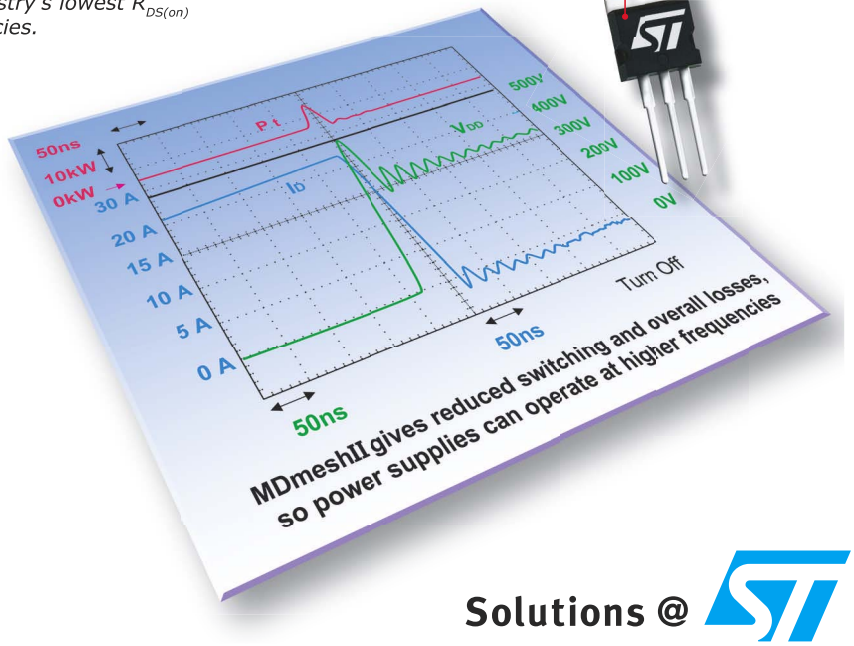
Part Number	V_{DSS} (@Tjmax)	$R_{DS(on)}$	ID	Pkge.
STB25NM60N-1	650V	< 0.170Ω	20A	I^2PAK
STF25NM60N	650V	< 0.170Ω	20A*	TO-220FP
STP25NM60N	650V	< 0.170Ω	20A	TO-220
STW25NM60N	650V	< 0.170Ω	20A	TO-247
STB25NM60N	650V	< 0.170Ω	20A	D^2PAK

* Limited only by maximum temperature allowed



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